

LVD-2002 SERVICE MANUAL

CONTENT

PART 1: Brief Introduction Of The LVD-2002

- ◆ Schematic Diagram
- ◆ Printed Circuit

PART 2: Exploded View

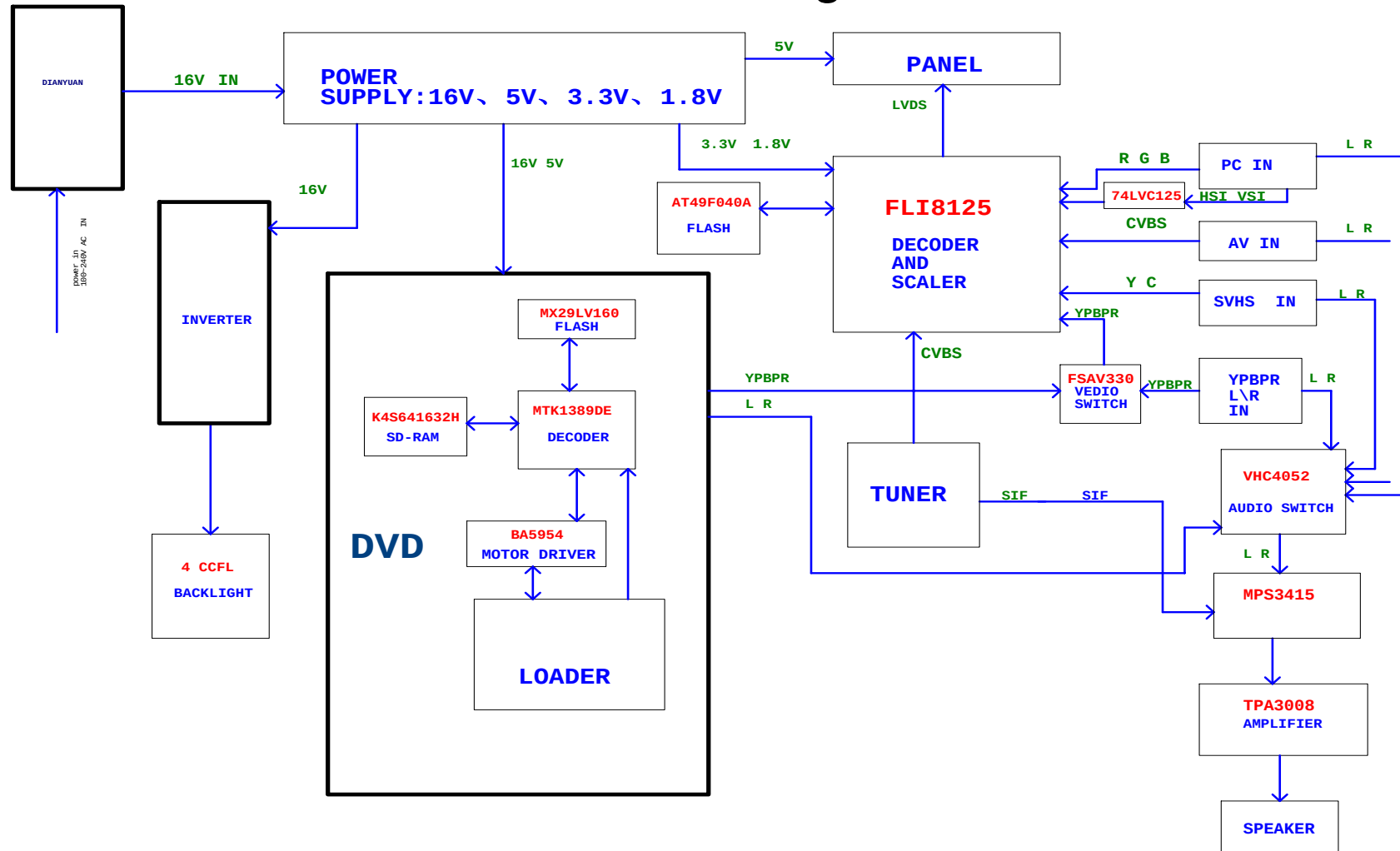
PART 3: Key Ics And Assemblies

PART 4: Detailed Circuit

- ◆ Main Board
- ◆ DVD Board
- ◆ Hi-voltage board

PART5: Debug Procedure

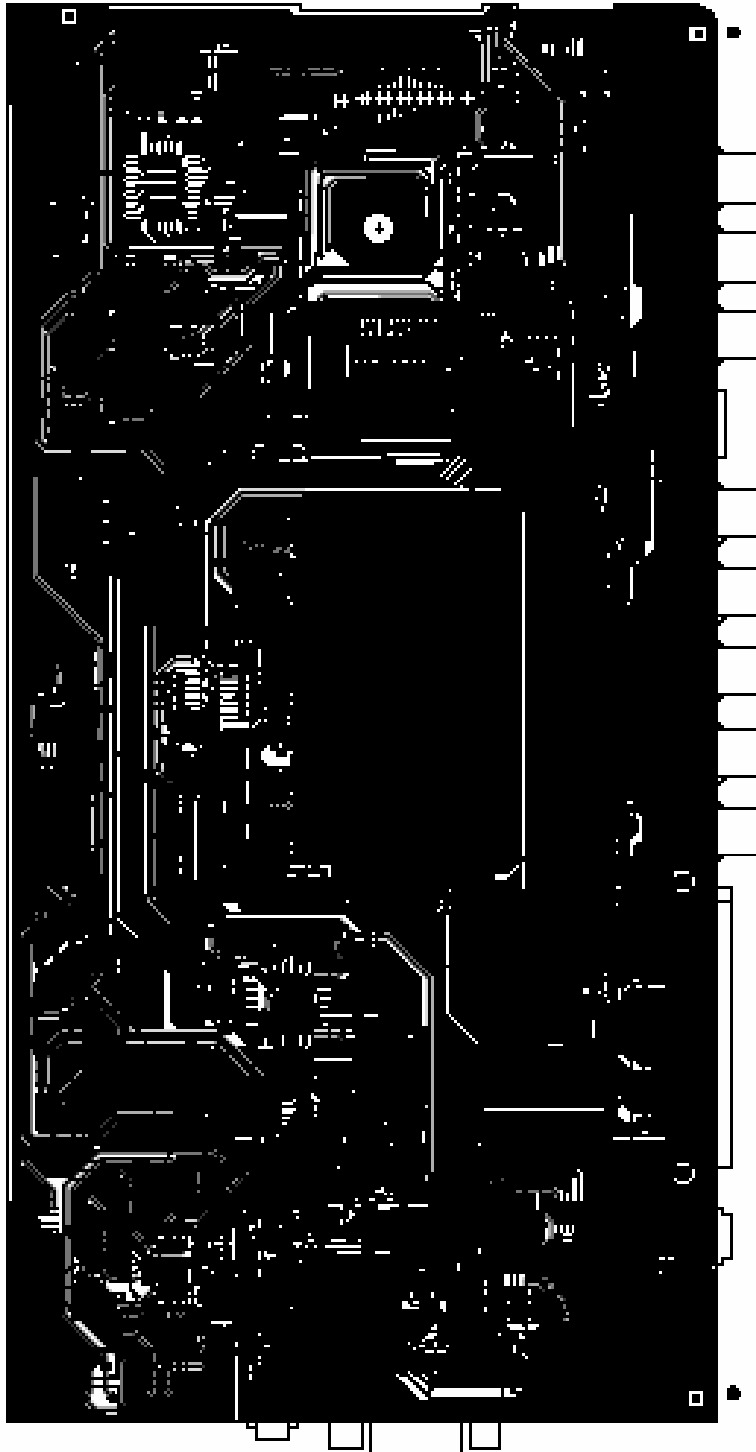
Part 1 Brief Introduction Of The LVD-2002 Schematic Diagram



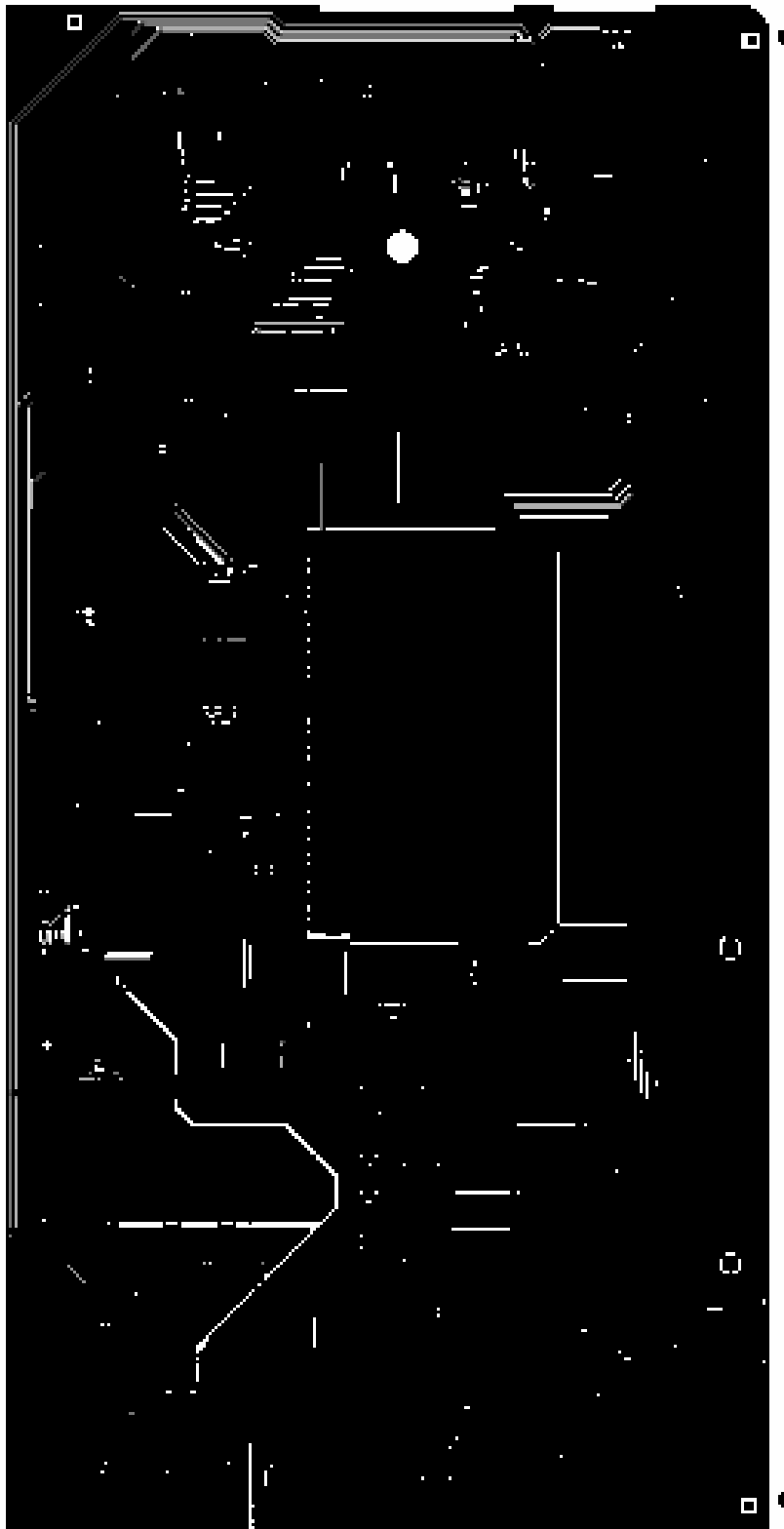
Printed Circuit

1. Main Board

A: TOP LAYER

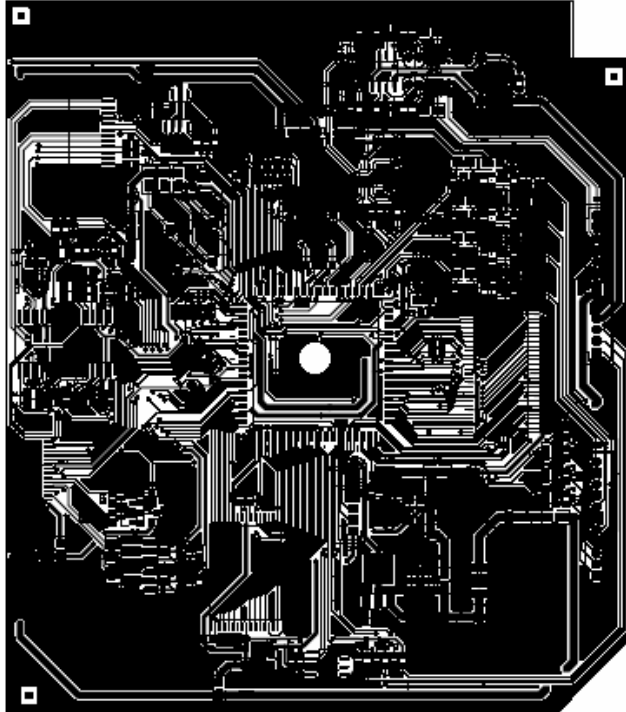


B: BOTTOM LAYER

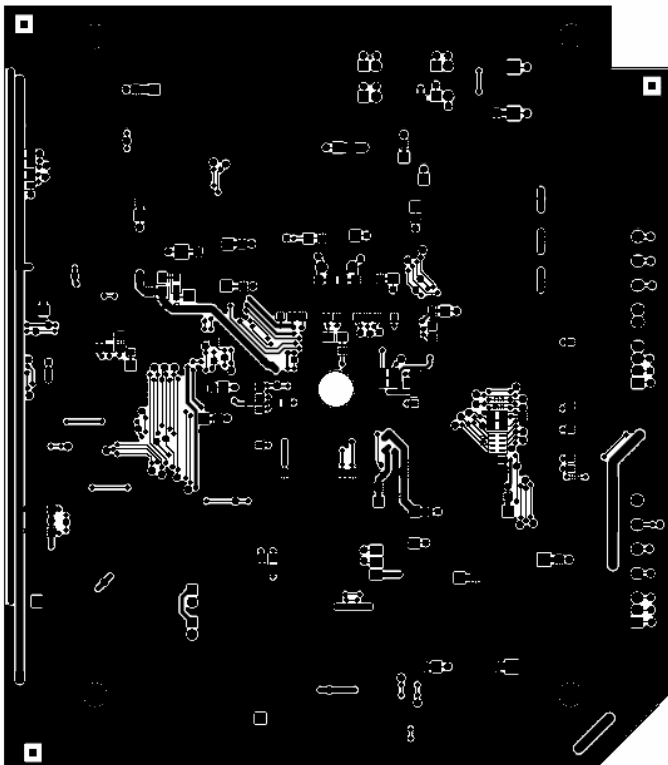


2. DVD Board

A: TOP LAYER

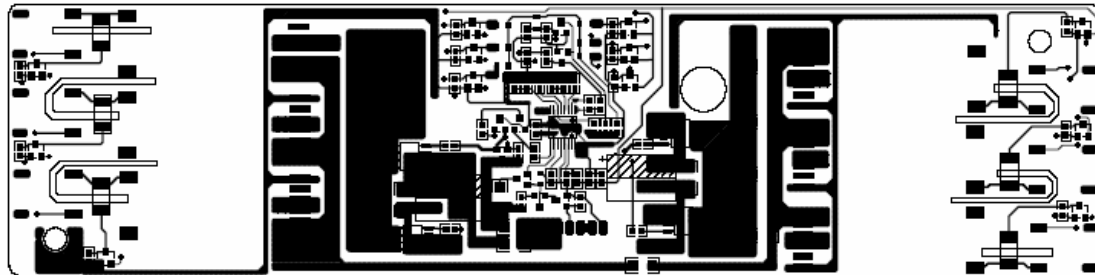


B: BOTTOM LAYER

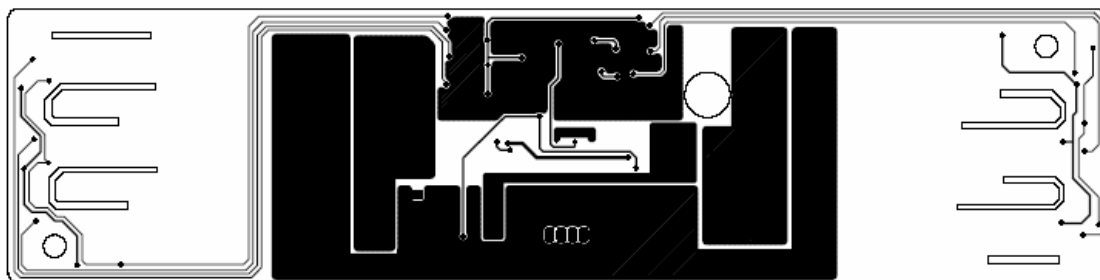


3. Inverter Board

A: TOP LAYER

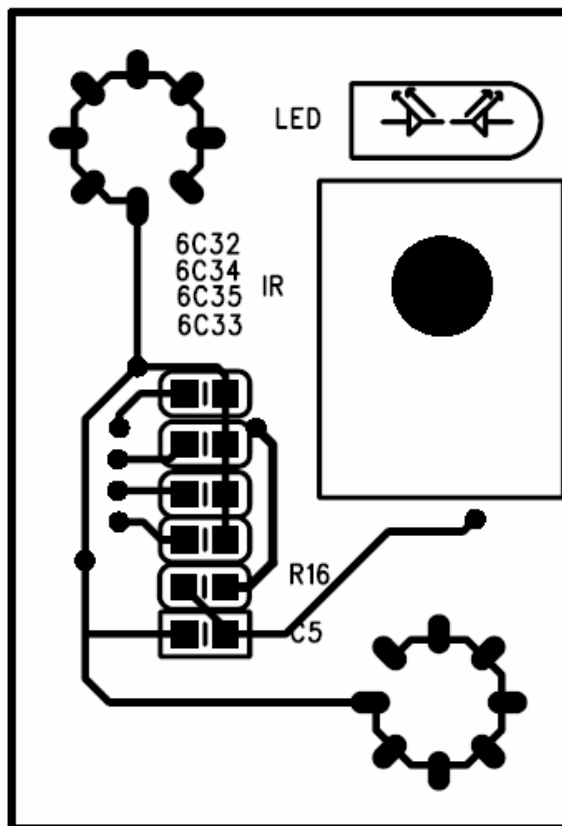


B: BOTTOM LAYER

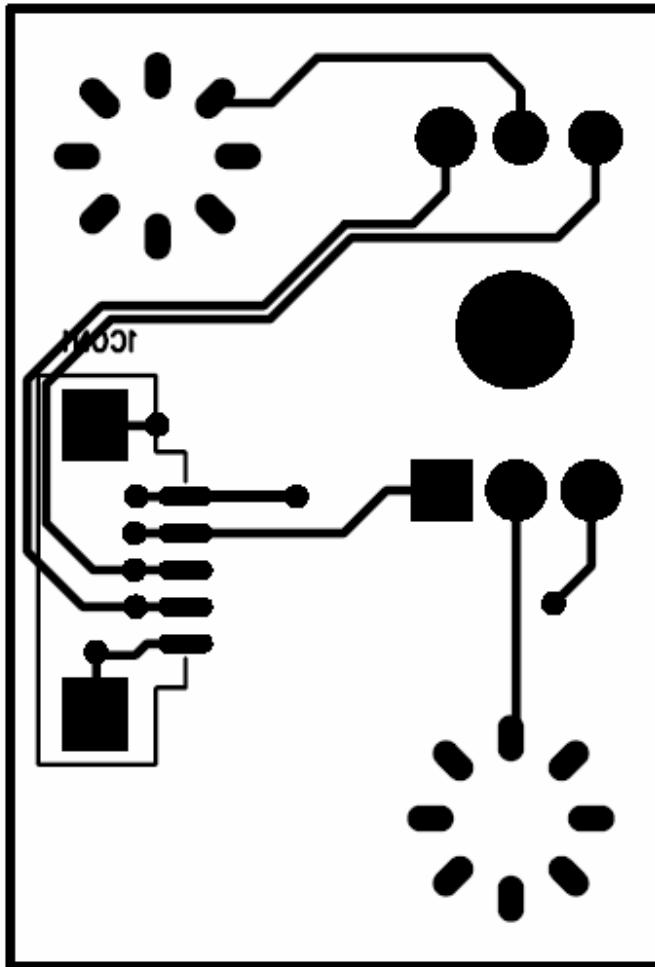


4. Remote Control Incept Board

A: TOP LAYER

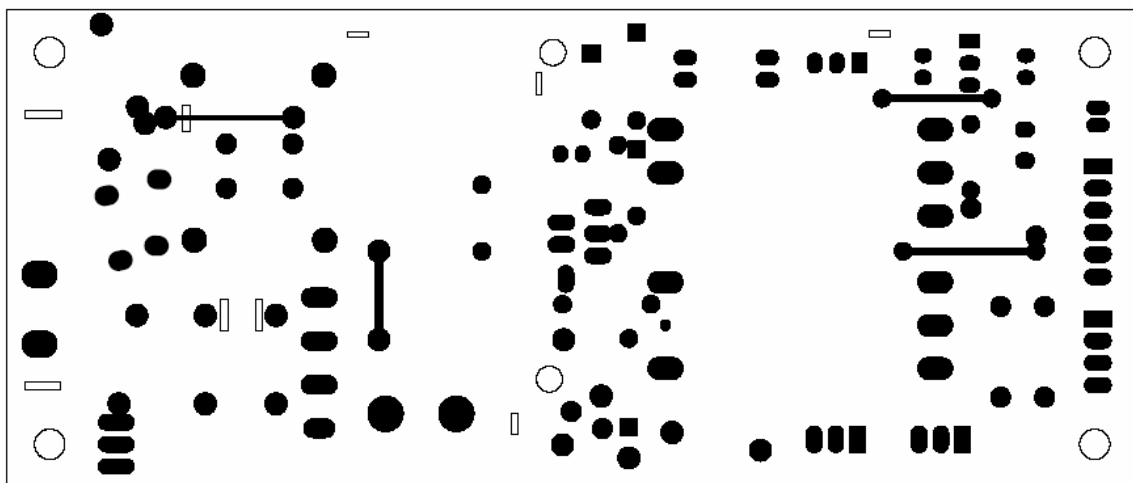


B: BOTTOM LAYER

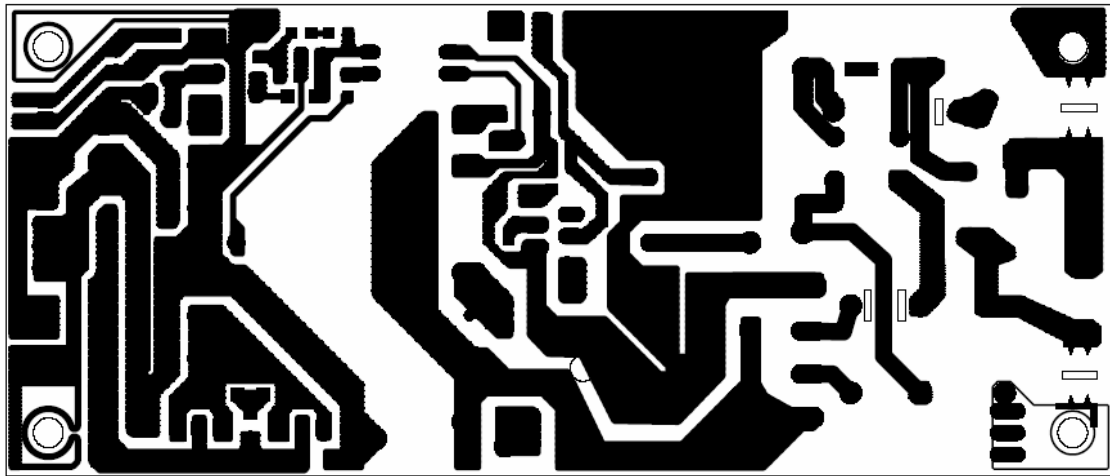


5. Power board

A: TOP LAYER

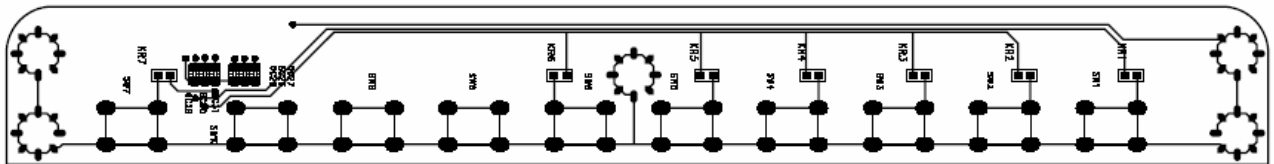


B: BOTTOM LAYER

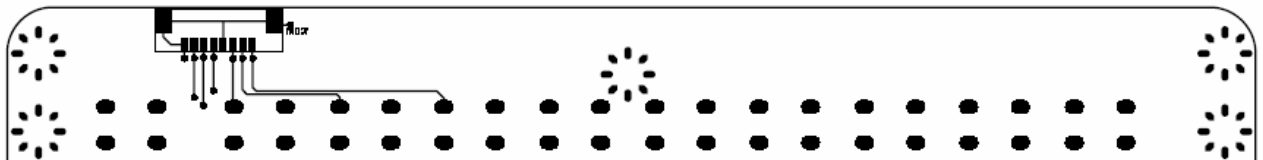


6. Key Board

A: TOP LAYER

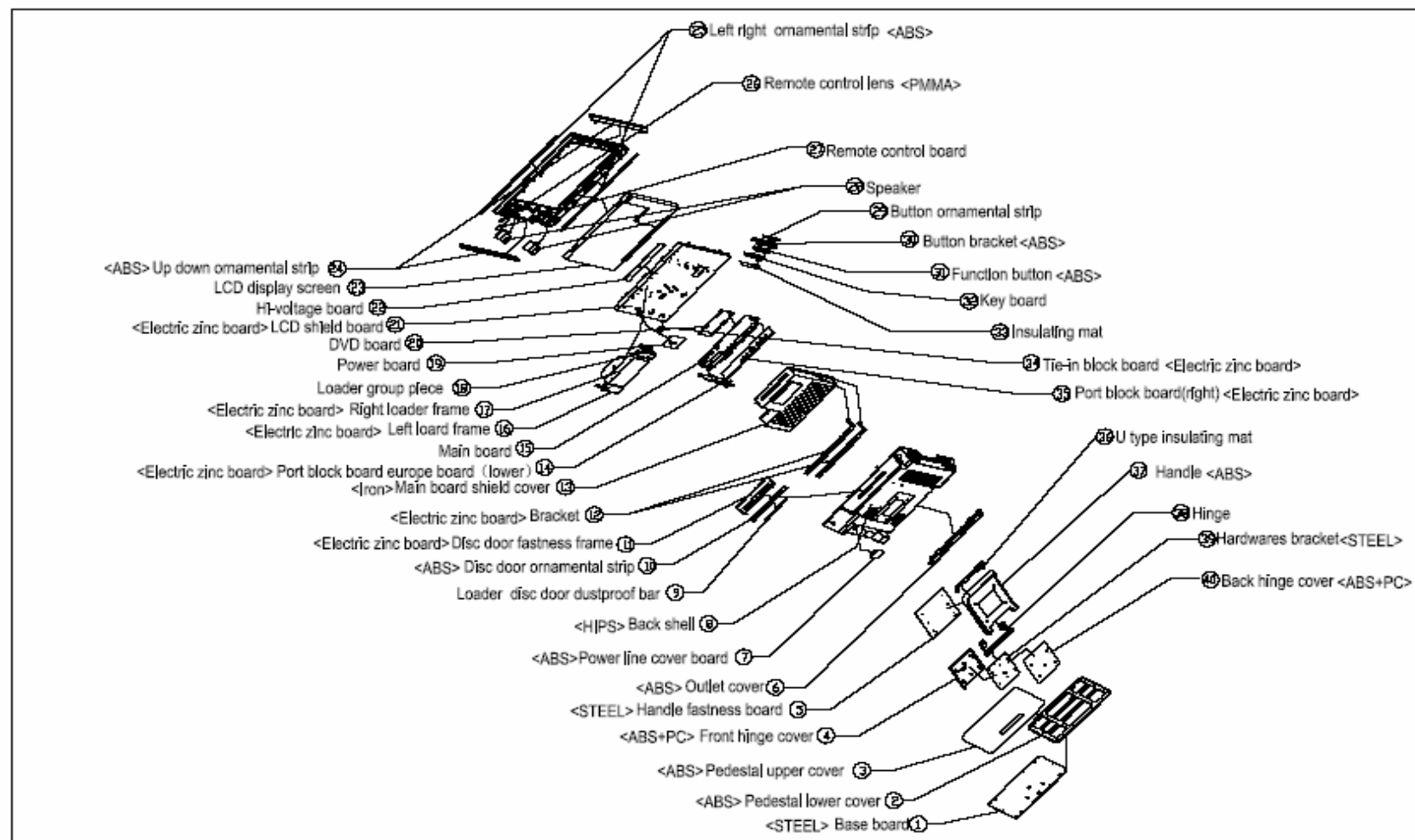


B: BOTTOM LAYER



Part 2 Exploded view

LVD-2002 exploded view



Spare Parts List (LVD-2002)

Item	Description	QTY	Part №
			(Код ЗЧД=Номер ЗЧД)
1	BASE BOARD		LVD-2002-1
2	PEDESTAL LOWER COVER		LVD-2002-2
3	PEDESTAL UPPER COVER		LVD-2002-3
4	FRONT HINGE COVER		LVD-2002-4
5	HANDLE FASTNESS BOARD		LVD-2002-5
6	OUTLET COVER		LVD-2002-6
7	POWER LINE COVER BOARD		LVD-2002-7
8	BACK SHELL		LVD-2002-8
9	LOADER DISC DOOR DUSTPROOF BAR		LVD-2002-9
10	DISC DOOR ORNAMENTAL STRIP		LVD-2002-10
11	DISC DOOR FASTNESS FRAME		LVD-2002-11
12	BRACKET		LVD-2002-12
13	MAIN BOARD SHIELD COVER		LVD-2002-13
14	PORT BLOCK EUROPE BOARD		LVD-2002-14
15	MAIN BOARD		LVD-2002-15
16	LEFT LOARD FRAME		LVD-2002-16
17	RIGHT LOADER FRAME		LVD-2002-17
18	LOADER GROUP PLECE		LVD-2002-18
19	POWER BOARD		LVD-2002-19
20	DVD BOARD		LVD-2002-20
21	LCD SHIELD BOARD		LVD-2002-21
22	HI-VOLTAGE BOARD		LVD-2002-22
23	LCD DISPLAY SCREEN		LVD-2002-23
24	UP DOWN OMAMENTAL STRIP		LVD-2002-24
25	LEFT RAIGHT ORNAMENTAL STRIP		LVD-2002-25
26	REMOTE CONTROL LENS		LVD-2002-26
27	REMOTE CONTROL BOARD		LVD-2002-27
28	SPEAKER		LVD-2002-28
29	BUTTON ORNAMENTAL STRIP		LVD-2002-29
30	BUTTON BRACKET		LVD-2002-30
31	FUNCTIONAL BUTTON		LVD-2002-31
32	KEY BOARD		LVD-2002-32
33	INSULATING MAT		LVD-2002-33
34	TIE-IN BLOCK BOARD		LVD-2002-34
35	PORT BLOCK BOARD		LVD-2002-35
36	U TUPE INSULATING MAT		LVD-2002-36
37	HANDLE		LVD-2002-37
38	HINGE		LVD-2002-38
39	HARDWARES BRACKET		LVD-2002-39
40	BACK HINGE COVER		LVD-2002-40
41	REMOTE CONTROL		LVD-2002-41

Part 3 Key ICS And Assemblies

On Main Board			On DVD board		
Serial No	Position	Type	Serial no	Position	Type
1	1U3	AP1513S	1	L31	BA033
2	2U1	MSP3415G	2	U3	AZ1117H-1.8
3	2U2	TPA3008D2PHP	3	U6	MT1389DE/E
4	4U1	24LC32	4	U4	BA5954
5	5U3	FSAV330	5	U5	BA6287
6	4U2	AT49BV040B	6	U8	IS42S16400B-7T
7	5U5	L7808C-V	7	U9	MX29LV160BBTC-70
8	4U3	FLI8125-LF	8	U7	24C16
9	5U4	CD4052	9	U11	NJM4558
10	1U4	LM1117MPS-1.8V	10	U10	CS4344
11	5U1 5U2 5U6 5U7 5U8 5U9 5U10	PESD5V0L5	On Hi-voltage board		
12	1U2	FDS9435	1	U1	BIT3713
13	4U4	24C02	2	Q8 Q10	AF4410N
14	4U5	BH3547F			
15	1U1 1U5	AP1510			

ICS ON MAIN BOARD

1. FDS9435A

Single P-Channel Enhancement Mode Field Effect Transistor

SO-8 P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

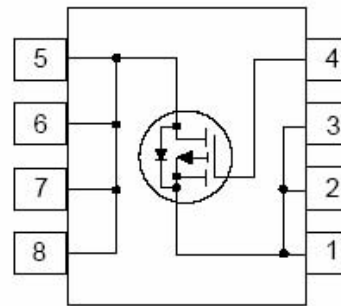
• Features

-5.3 A, -30 V, $R_{DS(ON)} = 0.045 \Omega$ @ $V_{GS} = -10$ V,

$R_{DS(ON)} = 0.075 \Omega$ @ $V_{GS} = -4.5$ V.

High density cell design for extremely low $R_{DS(ON)}$.

High power and current handling capability in a widely used surface mount package.



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDS9435A	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	-20	V
I_D	Drain Current - Continuous (Note 1a)	-5.3	A
	- Pulsed	-50	
P_D	Maximum Power Dissipation (Note 1a)	2.5	W
	(Note 1b)	1.2	
	(Note 1c)	1	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	$^\circ\text{C/W}$

2. FLI8125

The FLI8125 is a cost-effective, highly-integrated, mixed signal solution for TV and Digital Video applications. It incorporates a multi-standard video decoder, high-speed triple 8-bit Analog-to-Digital Converter(ADC),and front end switching. An integrated VBI Slicer adds Closed Captioning(CC) and Teletext service support, and the built-in microprocessor enables full system control without external devices.

Features

INTEGRATED TRIPLE ADC ▪ RGB / YPbPr support up to 135MHz ▪ SCART – RGB + Fast Blank support ▪ Interlaced and progressive scan ▪ External OSD support DIGITAL INPUT PORT ▪ 24-bit re-configurable input port INTEGRATED 2D VIDEO DECODER ▪ Worldwide NTSC/PAL/SECAM support ▪ Macrovision / VCR trick mode support EMBEDDED MICROPROCESSOR ▪ Turbo 186 core ▪ Internal RAM / ROM ▪ Serial Flash / Parallel ROM support ▪ 2-wire slave controller, UART support ▪ Internal RESET Controller ▪ GPIOs , Low Bandwidth ADC – 6 input ▪ Infra-red Interface SCALING ENGINE ▪ Independent H & V scaling factors ▪ 4:2:2 YPbPr or 4:4:4 RGB scaling ▪ Anamorphic scaling (non-linear)	FAROUDJA DCDI – EDGE™ ▪ Edge Correction – Eliminates objectionable stair-casing – Enhances clarity and realism ▪ Horizontal Enhancement ▪ Adaptive Contrast and Color (ACC) ▪ Active Color Management - II (ACM-II) DIGITAL OUTPUT ▪ 18/24-bit 85Mhz TTL output ▪ Dual LVDS up to SXGA ▪ Energy Spectrum Management for reducing EMI ▪ Programmable CLUT for gamma correction OSD CONTROLLER ▪ Up to 4 windows: 1, 2 or 4-bits per pixel color ▪ Programmable Font scalar to meet Teletext requirements VBI SLICER ▪ V-Chip, Closed Captioning, XDS, CGMS, WSS decode ▪ Teletext 1.5 support JTAG SUPPORT ▪ Boundary Scan support
--	---

• Pin Input



• Pin List

I/O Legend: A = Analog, I = Input, O = Output, P = Power, G= Ground

Table 1: Analog Input Port

Pin Name	No.	I/O	Description
VDD18_A B	158	AP	Analog Power (1.8V) for A & B Channels. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
NC	159		No Connection. Leave this pin open for normal operation.
GND18_C	160	AG	Analog Ground (1.8V Return) for C channel. Must be directly connected to the analog system ground plane on board.
VDD18_C	161	AP	Analog Power (1.8V) for C Channel. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
ADC_TES T	162	O	Analog Front End Test O/P. Leave this Pin open. Used for factory testing purpose only.
AVDD_AD C	163	AP	Analog Power (3.3V) for ADC. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
AGND	164	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
AGND	165	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
SV1P	166	AI	Positive analog sync input for channel 1. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	167	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.

A1P	168	AI	Positive analog input 'A' for channel 1. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	169	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
B1P	170	AI	Positive analog input 'B' for channel 1. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	171	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
C1P	172	AI	Positive analog input 'C' for channel 1. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
AVDD_A	173	AP	Analog Power (3.3V) for ADC of Channel-A. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
AN	174	AI	Negative analog input 'A' for channels 1 through 4. This acts as the return Path for the Sources connected to Channel-A Inputs. This has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network to Analog Ground Plane on board.
AGND	175	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
SV2P	176	AI	Positive analog sync input for channel 2. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	177	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
A2P	178	AI	Positive analog input 'A' for channel 2. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	179	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
B2P	180	AI	Positive analog input 'B' for channel 2. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	181	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
C2P	182	AI	Positive analog input 'C' for channel 2. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
AVDD_B	183	AP	Analog Power (3.3V) for ADC of Channel-B. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
BN	184	AI	Negative analog input 'B' for channels 1 through 4. This acts as the return Path for the Sources connected to Channel-B Inputs. This has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network to Analog Ground Plane on board.
AGND	185	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
SV3P	186	AI	Positive analog sync input for channel 3. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
VDD18_AB	158	AP	Analog Power (1.8V) for A & B Channels. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
GNDS	187	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
A3P	188	AI	Positive analog input 'A' for channel 3. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	189	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
B3P	190	AI	Positive analog input 'B' for channel 3. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	191	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
C3P	192	AI	Positive analog input 'C' for channel 3. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
AVDD_C	193	AP	Analog Power (3.3V) for ADC of Channel-C. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
CN	194	AI	Negative analog input 'C' for channels 1 through 4. This acts as the return Path for the Sources connected to Channel-C Inputs. This has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network to Analog Ground Plane on board.
AGND	195	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
SV4P	196	AI	Positive analog sync input for channel 4. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	197	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
A4P	198	AI	Positive analog input 'A' for channel 4. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	199	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
B4P	200	AI	Positive analog input 'B' for channel 4. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	201	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
C4P	202	AI	Positive analog input 'C' for channel 4. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
AVDD_SC	203	AP	Analog Power (3.3V) for ADC of SYNC Channel. Must be bypassed with 0.1uF capacitor to the analog system ground plane.

SVN	204	AI	Negative analog sync input for channels 1 through 4. This acts as the return Path for the Sources connected to SV Channel Inputs. This has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network to Analog Ground Plane on board.
VO_GND	205	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
VOOUT2	206	AO	Analog VOUT signal This is the Analog Video Output from the Decoder in the Composite Video format. This can be amplified and be fed to any video display device.
VDD18_SC	207	AP	Analog Power (1.8V) for SYNC Channel. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
GND18_SC	208	AG	Analog Ground (1.8V Return) for SYNC channel. Must be directly connected to the analog system ground plane on board.

Table 2: Low Bandwidth ADC Input Port

Pin Name	No	I/O	Description
VDDA33_LBADC	1	AP	Analog Power (3.3V) for Low Bandwidth ADC Block. Must be bypassed with 0.1uF capacitor.
LBADC_IN1	2	AI	Low Bandwidth Analog Input-1. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN2	3	AI	Low Bandwidth Analog Input-2. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN3	4	AI	Low Bandwidth Analog Input-3. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN4	5	AI	Low Bandwidth Analog Input-4. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN5	6	AI	Low Bandwidth Analog Input-5. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN6	7	AI	Low Bandwidth Analog Input-6. The Input signal connected to this Pin, must be bypassed with
LBADC_RTN	8	AG	This Pin provides the Return Path for LBADC inputs. Must be directly connected to the analog system ground plane on board.
VSSA33_LBADC	9	AG	Analog Ground for Low Bandwidth ADC Block. Must be directly connected to the analog system ground plane on board.

Table 3: RCLK PLL Pins

Pin Name	No	I/O	Description
GND_RPLL	11	DG	Digital GND for ADC clocking circuit. Must be directly connected to the digital system ground plane.
VDD_RPLL_18	12	DP	Digital power (1.8V) for ADC digital logic. Must be bypassed with capacitor to Ground Plane.
VBUFC_RPLL	13	O	Test Output. Leave this Pin Open. This is reserved for Factory Testing Purpose.
AGND_RPLL	14	AG	Analog ground for the Reference DDS PLL. Must be directly connected to the analog system ground plane.
XTAL	15	AO	Crystal oscillator output.
TCLK	16	AI	Reference clock (TCLK) from the 14.3MHz crystal oscillator.
AVDD_RPLL_33	17	AP	Analog Power (3.3V) for RCLK PLL. Must be bypassed with 0.1uF capacitor.

Table 4: Digital Video Input Port

Pin Name	No	I/O	Description
VID_CLK_1	153	I	Video port data clock input meant for Video Input – 1. Up to 75Mhz [Input, 5V-tolerant]
VIDIN_HS	122	I	When Video Input – 1 is in BT656 Mode, this Pin acts as Horizontal Sync Input for Video Input – 2. OR when Video Input – 1 is in 16 Bit Mode this Pin acts as Horizontal Sync Input for Video Input – 1. OR this Pin acts as Horizontal Sync Input for 24 Bit Video Input
VIDIN_VS	121	I	When Video Input – 1 is in BT656 Mode, this Pin acts as Vertical Sync Input for Video Input – 2. OR when Video Input – 1 is in 16 Bit Mode this Pin acts as Vertical Sync Input for Video Input – 1. OR this Pin acts as Vertical Sync Input for 24 Bit Video Input
VID_DATA_IN_0	135	IO	Input YUV data in 8-bit BT656 of Video Input – 1 [Bi-Directional, 5V-tolerant] OR Input Y Data in case of 16 Bit Video Input (CCIR601) of Video Input – 1 OR Input Red Data in case of 24 Bit Video Input
VID_DATA_IN_1	136		
VID_DATA_IN_2	137		
VID_DATA_IN_3	138		
VID_DATA_IN_4	139		
VID_DATA_IN_5	140		
VID_DATA_IN_6	141		
VID_DATA_IN_7	142		
Pin Name	No	I/O	Description

VID_DATA_IN_8	145	IO	Input Pr / Pb Data in case of 16 Bit Video Input (CCIR601) of Video Input – 1 OR Input Green Data in case of 24 Bit Video Input
VID_DATA_IN_9	146		
VID_DATA_IN_10	147		
VID_DATA_IN_11	148		
VID_DATA_IN_12	149		
VID_DATA_IN_13	150		
VID_DATA_IN_14	151		
VID_DATA_IN_15	152		
VID_DATA_IN_16	123	IO	Input Blue Data in case of 24 Bit Video Input OR Video Input – 2 in 8-bit with Embedded Sync / Separate Sync Sync in which case VID_DATA_IN_16 acts as the LSB of the 8-bit Video input and VID_DATA_IN_23 acts as the MSB of the 8-bit Video input.
VID_DATA_IN_17	124		
VID_DATA_IN_18	125		
VID_DATA_IN_19	128		
VID_DATA_IN_20	129		
VID_DATA_IN_21	130		
VID_DATA_IN_22	131		
VID_DATA_IN_23	132		
VID_CLK2	118	I	Video port data clock input meant for Video Input – 2. Up to 75Mhz [Input, 5V-tolerant]
VID_DE/FLD	115	I	Video Active Signal Input or the Field Signal Input from external Digital Video Source.

Note: In case of Multiple Digital Video Input Sources, only one source could be in 8-Bit with embedded Sync (BT656 mode) format.

Table 5: System Interface

Pin Name	No	I/O	Description
RESETn	10	I	Hardware Reset (active low) [Schmitt trigger, 5v-tolerant] Connect to ground with 0.01uF (or larger) capacitor.
TEST	20	I	For normal mode of operation connect this Pin to Ground.
GPIO15	21	IO	This pin is available as a general-purpose input/output port. Also it is optionally programmable to give out the external chip select signal meant for external SRAM. Refer to note below.
HSYNC2	22	I	Horizontal Sync signal Input-2. Used when Analog RGB component signal carries separate HSYNC signal.
VSYNC2	23	I	Vertical Sync signal Input-2. Used when Analog RGB component signal carries separate VSYNC signal.
HOST_SCLK	24	IO	Host input clock or 186 UART Data In or JTAG clock signal. [Input, Schmitt trigger, 5V-tolerant]
HOST_SDATA	25	IO	Host input data or 186 UART Data Out or JTAG mode signal. [Bi-directional, Schmitt trigger, slew rate limited, 5V-tolerant]
DDC_SCLK	26	IO	DDC2Bi clock for VGA Port [internal 10KΩ pull-up resistor]
DDC_SDATA	27	IO	DDC2Bi data for VGA Port [internal 10KΩ pull-up resistor]
MSTR_SCLK	30	O	Clock signal from Master Serial 2 Wire Interface Controller
MSTR_SDATA	31	IO	Data signal meant for Master Serial 2 Wire interface Controller
TCK	34	IO	This Pin accepts the Input Clock signal in case of Boundary Scan Mode.
TDI	35	IO	This Pin accepts the Input Data signal in case of Boundary Scan Mode.
TMS	36	IO	This Pin accepts the Input Test Mode Select signal in case of Boundary Scan Mode.
TRST	37	IO	This Pin accepts the Boundary Scan Reset signal in case of Boundary Scan Mode.
GPIO6/IRin	38	IO	Input from Infra Red Decoder can be connected to this Pin. When not used, this pin is available as General Purpose Input/output Port.
GPIO7/IRQin	41	IO	Input Interrupt Request signal can be connected to this Pin. When not used, this pin is available as General Purpose Input/output Port.
GPIO8/IRQout	42	IO	This Pin will give out the Interrupt Signal to interrupt external Micro. When not used, this pin is available as General Purpose Input/output Port.
GPIO9/SIPC_SCLK	43	IO	This Pin accepts the Clock signal from External Serial 2 Wire interface Bus if FLI8125 is programmed to be in Slave mode. When not used, this pin is available as General Purpose Input/output Port.
GPIO10/SIPC_SDATA/ A18	44	IO	This Pin acts as the Data I/O signal when used with External Serial 2 Wire interface Bus if FLI8125 is programmed to be in Slave mode. Or this Pin is programmable to give out Address # 18 from the Internal Micro when used with 512K External Memory. When not used, this pin is available as General Purpose Input/output Port.
GPIO11/PWM0	47	IO	This Pin can be programmed to give out Pulse Width Modulated Output Pulses for external use. When not used, this pin is available as General Purpose Input/output Port.
GPIO12/PWM1	48	IO	This Pin can be programmed to give out Pulse Width Modulated Output Pulses for external use. When not used, this pin is available as General Purpose Input/output Port.
GPIO13/PWM2	51	IO	This Pin can be programmed to give out Pulse Width Modulated Output Pulses for external use. When not used, this pin is available as General Purpose Input/output Port.
Pin Name	No	I/O	Description

GPIO14/PWM3/ SCART16	52	IO	This Pin can be programmed to give out Pulse Width Modulated Output Pulses for external use. Or it can be programmed to sense the Fast Blank Input signal from a SCART I/P source. When not used, this pin is available as General Purpose Input/output Port.
TDO	55	O	This Pin provides the Output Data in case of Boundary Scan Mode.
HSYNC1	156	I	Horizontal Sync signal Input-1. Used when Analog RGB component signal carries separate HSYNC signal.
VSYNC1	157	I	Vertical Sync signal Input-1. Used when Analog RGB component signal carries separate VSYNC signal.
101		O	Clock Output meant for External OSD Controller
102		O	Horizontal Sync Output meant for External OSD Controller
XOSD_CLK	103	O	Vertical Sync Output meant for External OSD Controller
XOSD_HS	104	O	Field Signal Output meant for External OSD Controller
PD20/B4/GPIO0	86	IO	These Pins provide the Panel Data as shown in the TTL Display Interface Table below. These are available as General Purpose Input / Output Pins when not used as Panel Data.
PD21/B5/GPIO1	87		
PD22/B6/GPIO2	88		
PD23/B7/GPIO3	89		

Table 6: LVDS Display Interface

Pin Name	No	I/O	Description
PBIAS	53	O	Panel Bias Control (backlight enable) [Tri-state output, 5V- tolerant]
PPWR	54	O	Panel Power Control [Tri-state output, 5V- tolerant]
AVDD_LV_33	56	DP	Digital Power for LVDS Block. Connect to digital 3.3V supply.
VCO_LV	57	O	Reserved. Output for Testing Purpose only at Factory.
AVSS_LV	58	G	Ground for LVDS outputs.
AVDD_OUT_LV_33	59	DP	Digital Power for LVDS outputs. Connect to digital 3.3V supply.
CH3P_LV_E	60	O	These form the Differential Data Output for Channel – 3 (Even).
CH3N_LV_E	61		
CLKP_LV_E	62	O	These form the Differential Clock Output Even Channel.
CLKN_LV_E	63		
CH2P_LV_E	64	O	These form the Differential Data Output for Channel – 2 (Even).
CH2N_LV_E	65		
CH1P_LV_E	66	O	These form the Differential Data Output for Channel – 1 (Even).
CH1N_LV_E	67		
CH0P_LV_E	68	O	These form the Differential Data Output for Channel – 0 (Even).
CH0N_LV_E	69		
AVSS_OUT_LV	70	G	Ground for LVDS outputs.
AVDD_OUT_LV_33	71	DP	Digital Power for LVDS outputs. Connect to digital 3.3V supply.
CH3P_LV_O	72	O	These form the Differential Data Output for Channel – 3 (Odd).
CH3N_LV_O	73		
CLKP_LV_O	74	O	These form the Differential Clock Output Odd Channel.
CLKN_LV_O	75		
CH2P_LV_O	76	O	These form the Differential Data Output for Channel – 2 (Odd).
CH2N_LV_O	77		
CH1P_LV_O	78	O	These form the Differential Data Output for Channel – 1 (Odd).
CH1N_LV_O	79		
CH0P_LV_O	80	O	These form the Differential Data Output for Channel – 0 (Odd).
CH0N_LV_O	81		
AVSS_OUT_LV	82	G	Ground for LVDS outputs.
AVDD_OUT_LV_33	83	DP	Digital Power for LVDS outputs. Connect to digital 3.3V supply.

Table 7: TTL Display Interface

Pin Name	No	I/O	Description For 8-bit panels	For 6-bit panels
PBIAS	53	O	Panel Bias Control (backlight enable) [Tri-state output, 5V- tolerant]	
PPWR	54	O	Panel Power Control [Tri-state output, 5V- tolerant]	
AVDD_LV_33	56	DP	Digital Power for TTL Block. Connect to digital 3.3V supply.	
VCO_LV	57	O	Reserved. Output for Testing Purpose only at Factory.	
AVSS_LV	58	G	Ground for TTL outputs.	
AVDD_OUT_LV_33	59	DP	Digital Power for TTL outputs. Connect to digital 3.3V supply.	
R0	60	O	Red channel bit 0 (Even)	Not used.
R1	61	O	Red channel bit 1 (Even)	Not used.
R2	62	O	Red channel bit 2 (Even)	Red channel bit 0 (Even)
R3	63	O	Red channel bit 3 (Even)	Red channel bit 1 (Even)
R4	64	O	Red channel bit 4 (Even)	Red channel bit 2 (Even)
R5	65	O	Red channel bit 5 (Even)	Red channel bit 3 (Even)
R6	66	O	Red channel bit 6 (Even)	Red channel bit 4 (Even)
R7	67	O	Red channel bit 7 (Even)	Red channel bit 5 (Even)
G0	68	O	Green channel bit 0 (Even)	Not used.
G1	69	O	Green channel bit 1 (Even)	Not used.
AVSS_OUT_LV	70	G	Ground for TTL outputs.	
AVDD_OUT_LV_33	71	DP	Digital Power for TTL outputs. Connect to digital 3.3V supply.	
G2	72	O	Green channel bit 2 (Even)	Green channel bit 0 (Even)
G3	73	O	Green channel bit 3 (Even)	Green channel bit 1 (Even)
G4	74	O	Green channel bit 4 (Even)	Green channel bit 2 (Even)
G5	75	O	Green channel bit 5 (Even)	Green channel bit 3 (Even)
G6	76	O	Green channel bit 6 (Even)	Green channel bit 4 (Even)
G7	77	O	Green channel bit 7 (Even)	Green channel bit 5 (Even)
B0	78	O	Blue channel bit 0 (Even)	Not used.
B1	79	O	Blue channel bit 1 (Even)	Not used.
B2	80	O	Blue channel bit 2 (Even)	Blue channel bit 0 (Even)
B3	81	O	Blue channel bit 3 (Even)	Blue channel bit 1 (Even)
AVSS_OUT_LV	82	G	Ground for TTL outputs.	
AVDD_OUT_LV_33	83	DP	Digital Power for TTL outputs. Connect to digital 3.3V supply.	
PD20/B4	86	O	Blue channel bit 4 (Even)	Blue channel bit 2 (Even)
PD21/B5	87	O	Blue channel bit 5 (Even)	Blue channel bit 3 (Even)
PD22/B6	88	O	Blue channel bit 6 (Even)	Blue channel bit 4 (Even)
PD23/B7	89	O	Blue channel bit 7 (Even)	Blue channel bit 5 (Even)
DEN	90	O	Display Data Enable	
DHS	91	O	Display Horizontal Sync.	
DVS	92	O	Display Vertical Sync.	
DCLK	93	O	Display Pixel Clock	
PD24	115	O	Red channel bit 0 (Odd)	Not used.
Pin Name	No	I/O	Description For 8-bit panels	For 6-bit panels
PD25	114	O	Red channel bit 1 (Odd)	Not used.
PD26	113	O	Red channel bit 2 (Odd)	Red channel bit 0 (Odd)
PD27	112	O	Red channel bit 3 (Odd)	Red channel bit 1 (Odd)
PD28	111	O	Red channel bit 4 (Odd)	Red channel bit 2 (Odd)
PD29	110	O	Red channel bit 5 (Odd)	Red channel bit 3 (Odd)
PD30	109	O	Red channel bit 6 (Odd)	Red channel bit 4 (Odd)
PD31	108	O	Red channel bit 7 (Odd)	Red channel bit 5 (Odd)
PD32	107	O	Green channel bit 0 (Odd)	Not used.
PD33	106	O	Green channel bit 1 (Odd)	Not used.
PD34	105	O	Green channel bit 2 (Odd)	Green channel bit 0 (Odd)
PD35	104	O	Green channel bit 3 (Odd)	Green channel bit 1 (Odd)
PD36	103	O	Green channel bit 4 (Odd)	Green channel bit 2 (Odd)
PD37	102	O	Green channel bit 5 (Odd)	Green channel bit 3 (Odd)
PD38	101	O	Green channel bit 6 (Odd)	Green channel bit 4 (Odd)
PD39	123	O	Green channel bit 7 (Odd)	Green channel bit 5 (Odd)
PD40	124	O	Blue channel bit 0 (Odd)	Not used.
PD41	125	O	Blue channel bit 1 (Odd)	Not used.
PD42	128	O	Blue channel bit 2 (Odd)	Blue channel bit 0 (Odd)
PD43	129	O	Blue channel bit 3 (Odd)	Blue channel bit 1 (Odd)
PD44	130	O	Blue channel bit 4 (Odd)	Blue channel bit 2 (Odd)
PD45	131	O	Blue channel bit 5 (Odd)	Blue channel bit 3 (Odd)

PD46	132	O	Blue channel bit 6 (Odd)	Blue channel bit 4 (Odd)
PD47	118	O	Blue channel bit 7 (Odd)	Blue channel bit 5 (Odd)

Note: In case of 24 Bit TTL Panels the RGB Odd Channel Outputs will not be used. In that case they can be made available for other purposes as Address & Data from On-Chip Micro or Digital Video Input Data.

Table 8: Parallel/Serial ROM Interface

Pin Name	No	I/O	Description
A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	95 96 100 101 102 103 104 105 106 107 108 109 110 111 112 113 114 115	O	256K x8 PROM Address. These pins also have bootstrap functionality. For serial SPI ROM interface: - ROM_ADDR17 will be Serial Clock (ROM_SCLK) - ROM_ADDR16 will be Serial Data Output (ROM_SDO) For 512K X 8 PROM, Address Signal A18 is available thru Pin # 44 which is GPIO10.
D7 D6 D5 D4 D3 D2 D1 D0	132 131 130 129 128 125 124 123	IO	External PROM data input.
ROM_OEN	118	O	External PROM data Output Enable.
ROM_SDI/ ROM_WEN	97	O	External PROM data Write Enable (for In-System-Programming of FLASH) or Serial Data Input (SDI) for SPI ROM interface.
ROM_SCSN/ ROM_CSN	94	O	External PROM data Chip Select or Serial PROM Chip Select (ROM_SCSN) for SPI ROM interface.

Table 9: Digital Power and Ground

Pin Name	No	I/O	Description
RVDD_3.3	32 49 98 116 154	P	Ring VDD. Connect to digital 3.3V.
CVDD_1.8	18 28 39 45 84 119 126 133 143	P	Core VDD. Connect to digital 1.8V.
CRVSS	19 29 33 40 46 50 85 99 117 120 127 134 144 155	G	Chip ground for core and ring.

Table 10: JTAG Boundary Scan

Pin Name	No	I/O	Description
TCK	34	I	JTAG Boundary Scan TCK signal
TDO	55	O	JTAG Boundary Scan TDO signal
TDI	35	I	JTAG Boundary Scan TDI signal. Pad has internal 50K pull-up resistor.
TMS	36	I	JTAG Boundary Scan RST signal. Pad has internal 50K pull-up resistor.
TRST	37	I	JTAG Boundary Scan TMS signal. Pad has internal 50K pull-up resistor.

3. LM1117

FEATURES

- Output Current up to 1 A
- Low Dropout Voltage (700mV at 1A Output Current)
- Three Terminal Adjustable or Fixed 1.5V, 1.8V, 2.5V, 2.85V, 3.0V, 3.3V, 5.0V
- 2.85V Device for SCSI-II Active Terminator
- 0.04% Line Regulation, 0.1% Load Regulation
- Very Low Quiescent Current
- Internal Current and Terminal Limit
- Logic-Controlled Electronics Shutdown
- Surface Mount Package SOT-223 & TO-263 (D2-Pack)
- 100% Thermal Limit Burn-In

APPLICATION

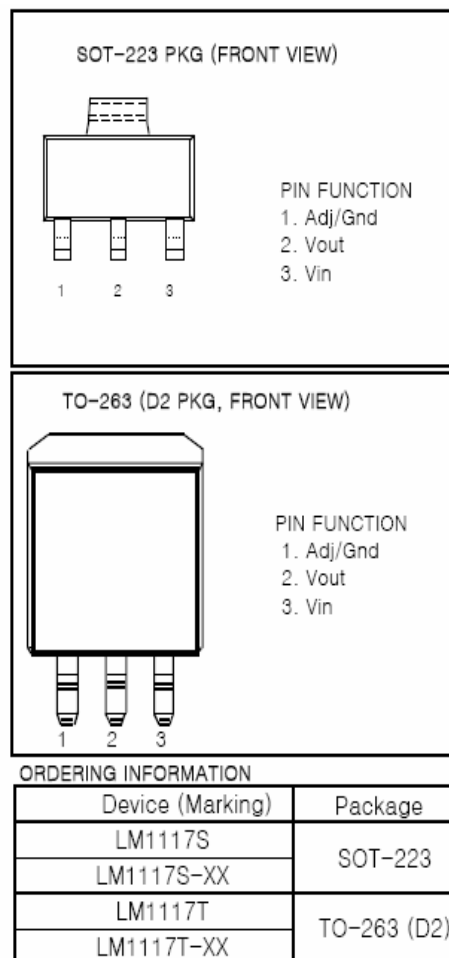
- Active SCSI Terminators
- Portable/Plan Top/Notebook Computers
- High Efficiency Linear Regulators
- SMPS Post Regulators
- Mother B/D Clock Supplies
- Disk Drives
- Battery Chargers

DESCRIPTION

The LM1117 is a low power positive-voltage regulator designed to meet 1A output current and comply with SCSI-II specifications with a fixed output voltage of 2.85V. This device is an excellent choice for use in battery-powered applications, as active terminators for the SCSI bus, and portable computers.

The LM1117 features very low quiescent current and very low dropout voltage of 700mV at a full load and lower as output current decreases. LM1117 is available as an adjustable or fixed 1.5V, 1.8V, 2.5V, 2.85V, 3.0V, 3.3V, and 5.0V output voltages.

The LM1117 is offered in a 3-pin surface mount package SOT-223 & TO-263. The output capacitor of 10 μ F or larger is needed for output stability of LM1117 as required by most of the other regulator circuits.



(X=Output Voltage=1.5V, 1.8V, 2.5V, 2.85V, 3.0V, 3.3V, 5.0V, Adjustable=AD)

4. TPA3008D2

10-W STEREO CLASS-D AUDIO POWER AMPLIFIER.

FEATURES

- 10-W/Channel Into an 16- Ω Load From a 17-V Supply
- Up to 92% Efficient, Class-D Operation Eliminates Need For Heatsinks
- 8.5-V to 18-V Single-Supply Operation
- Four Selectable, Fixed Gain Settings
- Differential Inputs Minimizes Common-Mode Noise
- Space-Saving, Thermally Enhanced PowerPAD™ Packaging
- Thermal and Short-Circuit Protection With Auto Recovery Option
- Pinout Similar to TPA3000D Family

DESCRIPTION

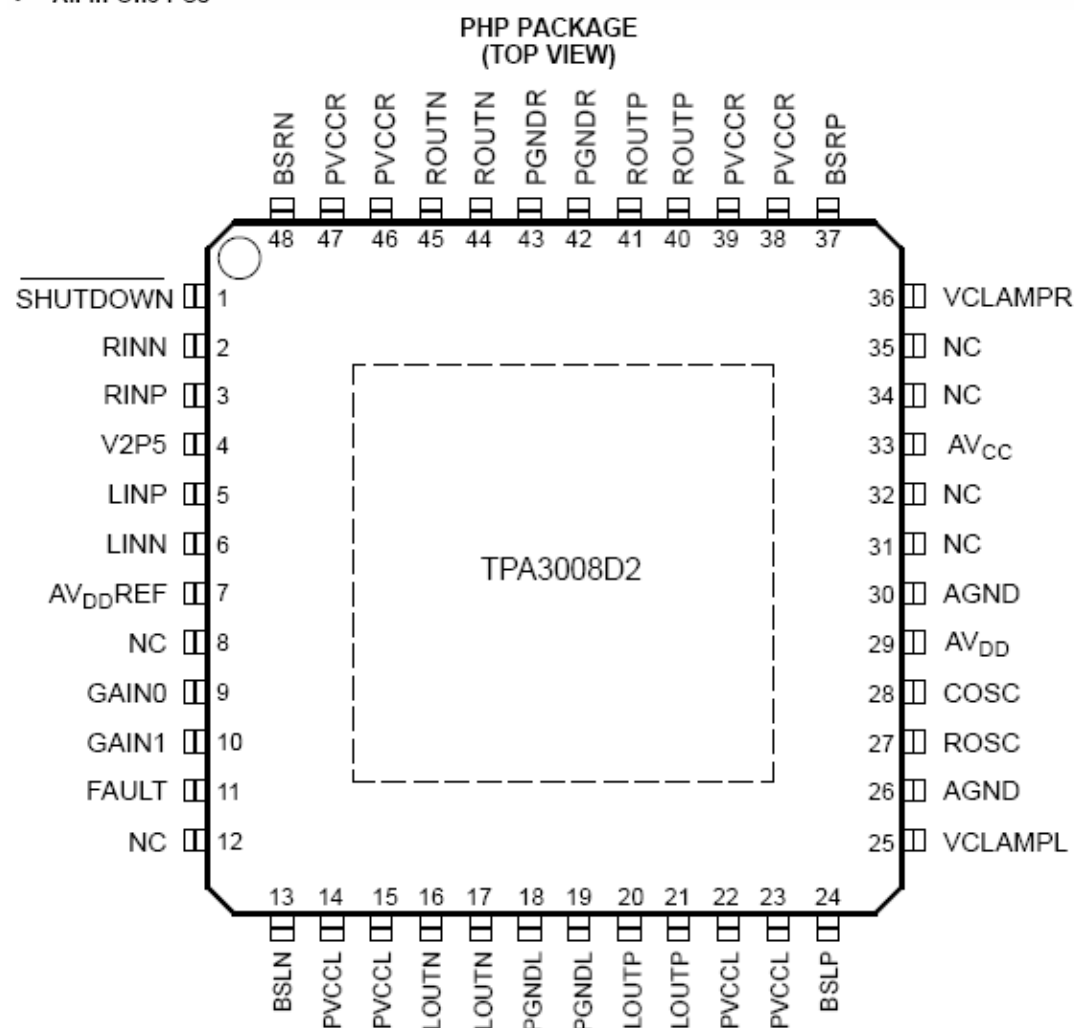
The TPA3008D2 is a 10-W (per channel) efficient, class-D audio amplifier for driving bridged-tied stereo speakers. The TPA3008D2 can drive stereo speakers as low as 8 Ω . The high efficiency of the TPA3008D2 eliminates the need for external heatsinks when playing music.

The gain of the amplifier is controlled by two gain select pins. The gain selections are 15.3, 21.2, 27.2, and 31.8 dB.

The outputs are fully protected against shorts to GND, VCC, and output-to-output shorts. A fault terminal allows short-circuit fault reporting and automatic recovery. Thermal protection ensures that the maximum junction temperature is not exceeded.

APPLICATIONS

- LCD Monitors and TVs
- All-In-One PCs



• Pin Description

TERMINAL FUNCTIONS

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
AGND	26, 30	-	Analog ground for digital/analog cells in core
AV _{CC}	33	-	High-voltage analog power supply, not connected internally to PVCCR or PVCLL
AV _{DD}	29	O	5-V Regulated output for use by internal cells and GAIN0, GAIN1 pins only. Not specified for driving other external circuitry.
AV _{DD} REF	7	O	5-V Reference output—connect to gain setting resistor or directly to GAIN0, GAIN1.
BSLN	13	-	Bootstrap I/O for left channel, negative high-side FET
BSLP	24	-	Bootstrap I/O for left channel, positive high-side FET
BSRN	48	-	Bootstrap I/O for right channel, negative high-side FET
BSRP	37	-	Bootstrap I/O for right channel, positive high-side FET
COSC	28	I/O	I/O for charge/discharging currents onto capacitor for ramp generator.
FAULT	11	O	Short-circuit detect fault output. FAULT = high, short-circuit detected. FAULT = low, normal operation. Status is reset when power is cycled or SHUTDOWN is cycled.
GAIN0	9	I	Gain select least significant bit. TTL logic levels with compliance to AV _{DD} .
GAIN1	10	I	Gain select most significant bit. TTL logic levels with compliance to AV _{DD} .
LINN	6	I	Negative audio input for left channel
LINP	5	I	Positive audio input for left channel
LOUTN	16, 17	O	Class-D 1/2-H-bridge negative output for left channel
LOUTP	20, 21	O	Class-D 1/2-H-bridge positive output for left channel
NC	8, 12, 31, 32, 34, 35	-	No internal connection
PGNDL	18, 19	-	Power ground for left channel H-bridge
PGNDR	42, 43	-	Power ground for right channel H-bridge
PVCLL	14, 15	-	Power supply for left channel H-bridge (internally connected to pins 22 and 23), not connected to PVCCR or AV _{CC} .
PVCLL	22, 23	-	Power supply for left channel H-bridge (internally connected to pins 14 and 15), not connected to PVCCR or AV _{CC} .
PVCCR	38, 39	-	Power supply for right channel H-bridge (internally connected to pins 46 and 47), not connected to PVCLL or AV _{CC} .
PVCCR	46, 47	-	Power supply for right channel H-bridge (internally connected to pins 38 and 39), not connected to PVCLL or AV _{CC} .
RINP	3	I	Positive audio input for right channel
RINN	2	I	Negative audio input for right channel
ROSC	27	I/O	I/O current setting resistor for ramp generator.
ROUTN	44, 45	O	Class-D 1/2-H-bridge negative output for right channel
ROUTP	40, 41	O	Class-D 1/2-H-bridge positive output for right channel
SHUTDOWN	1	I	Shutdown signal for IC (low = shutdown, high = operational). TTL logic levels with compliance to V _{CC} .
VCLAMPL	25	-	Internally generated voltage supply for left channel bootstrap capacitors.
VCLAMPR	36	-	Internally generated voltage supply for right channel bootstrap capacitors.
V2P5	4	O	2.5-V Reference for analog cells.
Thermal Pad	-	-	Connect to AGND and PGND—should be the center point for both grounds. Internal resistive connection to AGND.

5. FSAV330

Low On Resistance Quad SPDT Wide Bandwidth Video Switch

General Description

The Fairchild Video Switch FSAV330 is a quad single pole/double throw high-speed CMOS TTL-compatible video switch. The low On Resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

When $\overline{OE}$ is LOW, the select pin connects the A Port to the selected B Port output. When $\overline{OE}$ is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Features

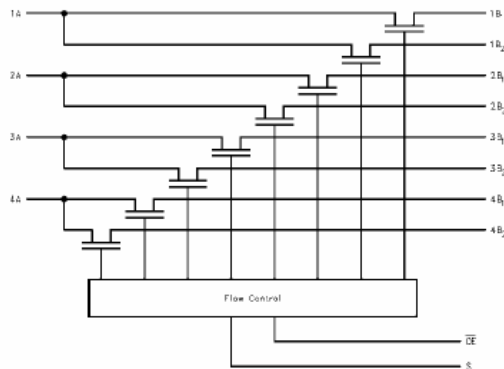
- Replacement for the P15V330
- Wide bandwidth 180 MHz
- 4Ω switch connection between two ports
- Minimal propagation delay through the switch
- Low I_{CC}
- Zero bounce in flow-through mode
- Control inputs compatible with TTL level

Ordering Code:

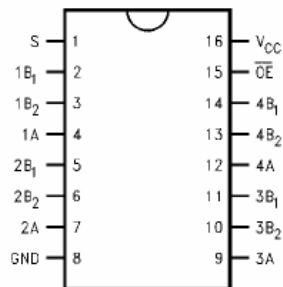
Order Number	Package Number	Package Description
FSAV330M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
FSAV330QSC	MQA16	16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
FSAV330MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Pin Descriptions

Pin Name	Description
$\overline{OE}$	Bus Switch Enable
S	Select Input
A	Bus A
B ₁ -B ₂	Bus B

Truth Table

S	$\overline{OE}$	Function
X	H	Disconnect
L	L	A = B ₁
H	L	A = B ₂

6. CD4052B

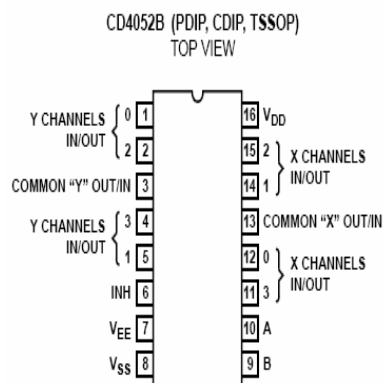
The CD4052B is a differential 4-Channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

Features

- Wide Range of Digital and Analog Signal Levels
 - Digital 3V to 20V
 - Analog $\leq 20V_{p-p}$
- Low ON Resistance, 125 Ω (Typ) Over 15V_{p-p} Signal Input Range for $V_{DD}-V_{EE} = 18V$
- High OFF Resistance, Channel Leakage of $\pm 100pA$ (Typ) at $V_{DD}-V_{EE} = 18V$
- Logic-Level Conversion for Digital Addressing Signals of 3V to 20V ($V_{DD}-V_{SS} = 3V$ to 20V) to Switch Analog Signals to 20V_{p-p} ($V_{DD}-V_{EE} = 20V$)
- Matched Switch Characteristics, $r_{ON} = 5\Omega$ (Typ) for $V_{DD}-V_{EE} = 15V$
- Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2 μW (Typ) at $V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10V$
- Binary Address Decoding on Chip
- 5V, 10V and 15V Parametric Ratings
- 10% Tested for Quiescent Current at 20V
- Maximum Input Current of 1 μA at 18V Over Full Package Temperature Range, 100nA at 18V and 25°C
- Break-Before-Make Switching Eliminates Channel Overlap

Applications

- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Signal Gating
- **Pinouts**



7. AP1513

■ Features

- Input voltage: 3.6V to 18V.
- Output voltage: 0.8V to V_{CC} .
- Duty ratio: 0% to 100% PWM control
- Oscillation frequency: 300KHz typ.
- Soft-start, Current limit, Enable function
- Thermal Shutdown function
- Built-in internal SW P-channel MOS
- SOP-8L **Pb-Free** Package.

■ Applications

- PC Motherboard
- LCD Monitor
- Graphic Card
- DVD-Video Player
- Telecom Equipment
- ADSL Modem
- Printer and other Peripheral Equipment
- Microprocessor core supply
- Networking power supply

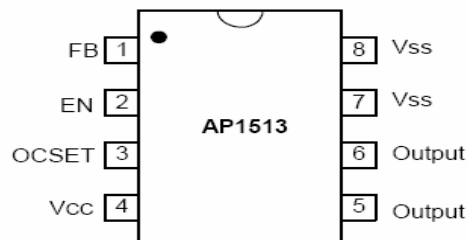
■ General Description

AP1513 consists of step-down switching regulator with PWM control. These devices include a reference voltage source, oscillation circuit, error amplifier, internal PMOS and etc.

AP1513 provides low-ripple power, high efficiency, and excellent transient characteristics. The PWM control circuit is able to vary the duty ratio linearly from 0 up to 100%. This converter also contains an error amplifier circuit as well as a soft-start circuit that prevents overshoot at startup. An enable function, an over current protect function and a short circuit protect function are built inside, and when OCP or SCP happens, the operation frequency will be reduced from 300KHz to 30KHz. Also, an internal compensation block is built in to minimum external component count.

With the addition of an internal P-channel Power MOS, a coil, capacitors, and a diode connected externally, these ICs can function as step-down switching regulators. They serve as ideal power supply units for portable devices when coupled with the SOP-8L mini-package, providing such outstanding features as low current consumption. Since this converter can accommodate an input voltage of up to 18V, it is also ideal when operating via an AC adapter.

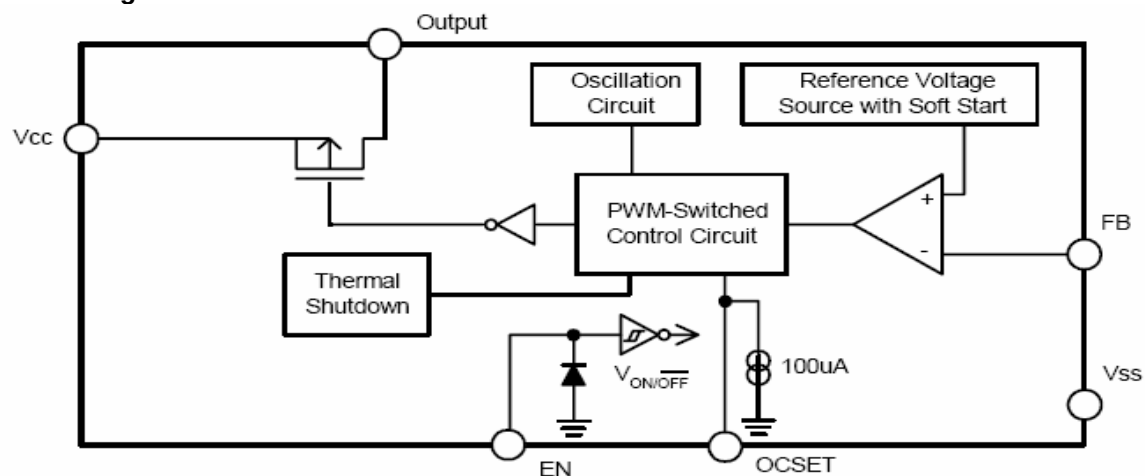
■ Pin Assignments



■ Pin Descriptions

Name	Pin	Description
FB	1	Feedback pin.
EN	2	Power-off pin H: Normal operation (Step-down operation) L: Step-down operation stopped (All circuits deactivated)
OCSET	3	Add an external resistor to set max output current.
Vcc	4	IC power supply pin
Output	5 ~ 6	Switch Pin. Connect external inductor/diode here. Minimize trace area at this pin to reduce EMI.
Vss	7 ~ 8	GND Pin

Block Diagram



8. AT49BV040B

Features

- Single Supply for Read and Write: 2.7V to 5.5V
- Fast Read Access Time – 70 ns ($V_{CC} = 2.7V$ to 3.6V); 55 ns ($V_{CC} = 4.5V$ to 5.5V)
- Internal Program Control and Timer
- Flexible Sector Architecture
 - One 16K Bytes Boot Sector with Programming Lockout
 - Two 8K Bytes Parameter Sectors
 - Eight Main Memory Sectors (One 32K Bytes, Seven 64K Bytes)
- Fast Erase Cycle Time – 8 Seconds
- Byte-by-Byte Programming – 10 μ s/Byte Typical
- Hardware Data Protection
- $\overline{DATA}$ Polling or Toggle Bit for End of Program Detection
- Low Power Dissipation
 - 20 mA Active Current
 - 25 μ A CMOS Standby Current for $V_{CC} = 2.7V$ to 3.6V
 - 30 μ A CMOS Standby Current for $V_{CC} = 4.5V$ to 5.5V
- Minimum 100,000 Write Cycles

Description

The AT49BV040B is a 2.7V to 5.5V in-system reprogrammable Flash Memory. Its 4 megabits of memory is organized as 524,288 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers an access time of 70 ns ($V_{CC} = 2.7V$ to 3.6V) and an access time of 55 ns ($V_{CC} = 4.5V$ to 5.5V). The power dissipation over the industrial temperature range with $V_{CC} = 2.7V$ to 3.6V is 72 mW and is 110 mW with $V_{CC} = 4.5V$ to 5.5V.

When the device is deselected, the CMOS standby current is less than 30 μ A. To allow for simple in-system reprogrammability, the AT49BV040B does not require high input voltages for programming. Reading data out of the device is similar to reading from an EPROM; it has standard $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ inputs to avoid bus contention. Reprogramming the AT49BV040B is performed by erasing a sector of data and then programming on a byte by byte basis. The byte programming time is a fast 10 μ s. The end of a program or erase cycle can be optionally detected by the $\overline{DATA}$ polling or toggle bit feature. Once the end of a byte program cycle has been detected, a new access for a read or program can begin. The typical number of program and erase cycles is in excess of 100,000 cycles.

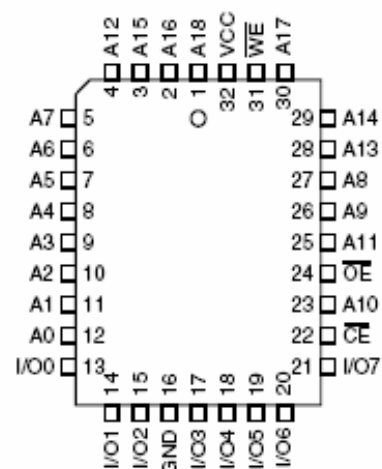
The device is erased by executing a chip erase or a sector erase command sequence; the device internally controls the erase operations. The memory array of the AT49BV040B is organized into two 8K byte parameter sectors, eight main memory sectors, and one boot sector.

The device has the capability to protect the data in the boot sector; this feature is enabled by a command sequence. The 16K-byte boot sector includes a reprogramming lock out feature to provide data integrity. The boot sector is designed to contain user secure code, and when the feature is enabled, the boot sector is permanently protected from being reprogrammed.

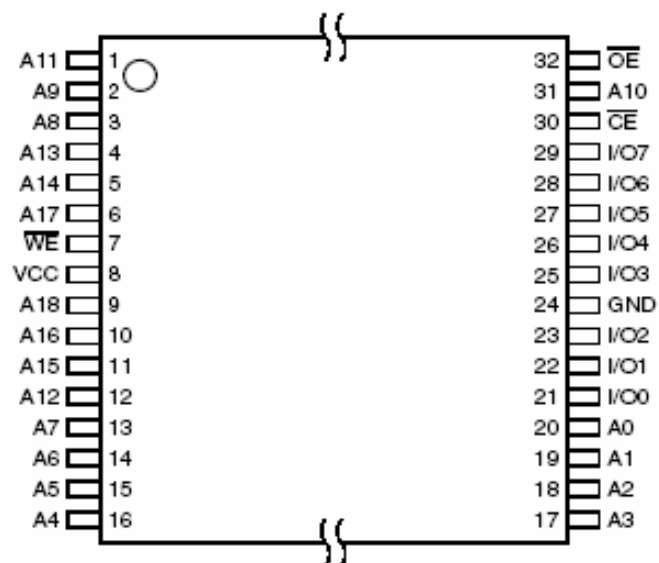
Pin Configurations

Pin Name	Function
A0 - A18	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs

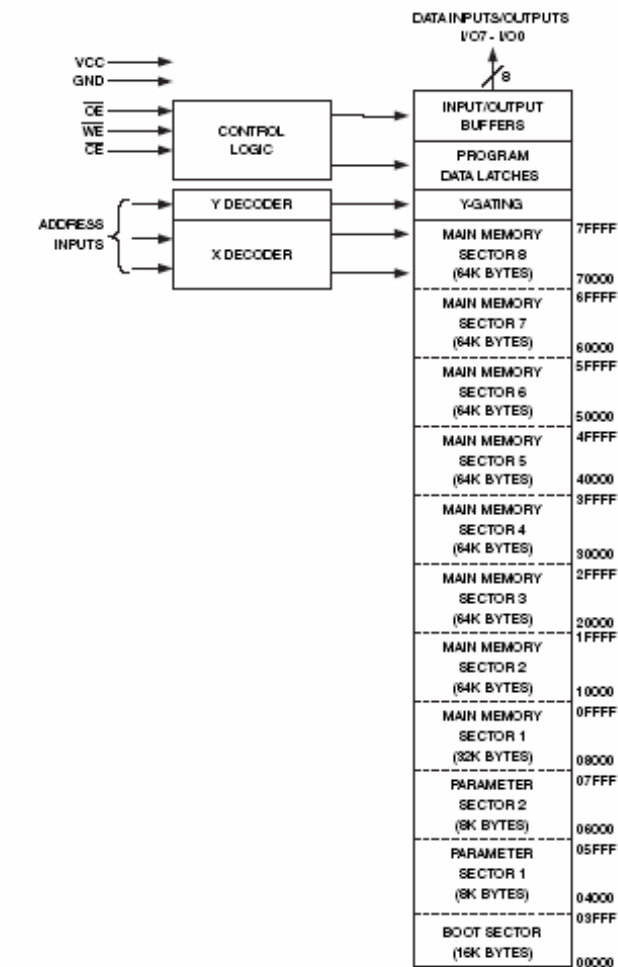
32-lead PLCC Top View



32-lead VSOP or 32-lead TSOP Top View – Type 1



Block Diagram



ICS ON DVD BOARD

1. BA5954

The AM5954 is a four-channel BTL driver IC for driving the motors and actuators such as used in CD-ROM drives. Two of the channels use current feedback to minimize the current phase shift caused by the influence of loading inductance.

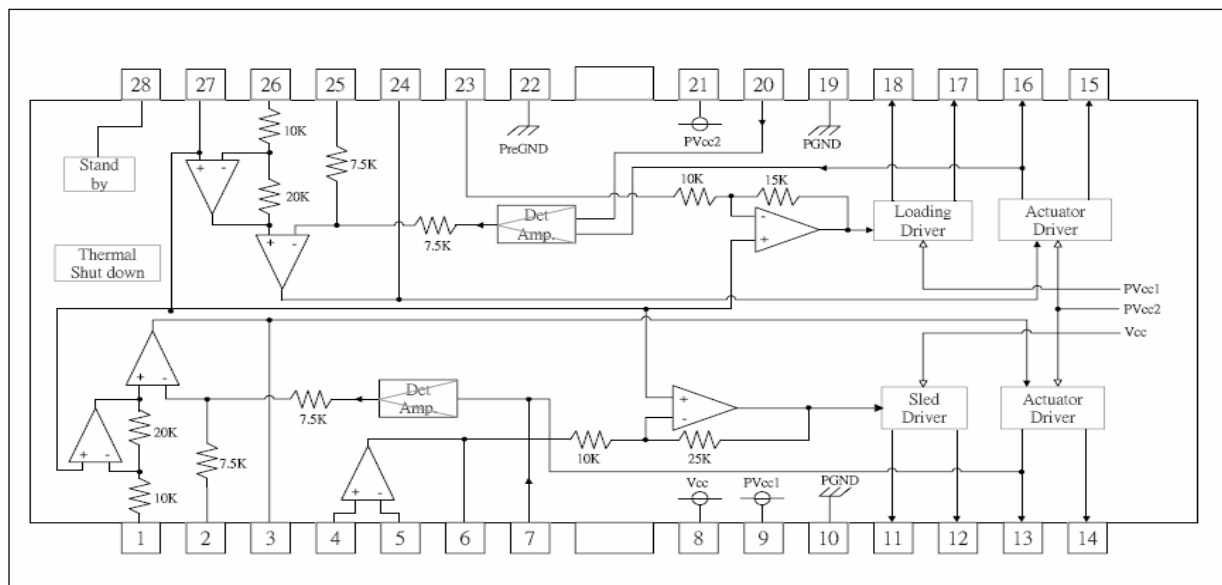
● Applications

BTL driver for CD, CD-ROM and DVD.

● Features

- 1) Two channels are current-type BTL drivers for actuators for tracking and focus, two channels are voltage-type BTL driver for sled and loading motors.
- 2) Wide dynamic range [9.0V(*typ*) when $V_{cc}=PV_{cc}=12V$, at $R_L=8\Omega$ load].
- 3) Separating power of V_{cc} and PV_{cc} to improve power efficiency by a low supply voltage for tracking and focus.
- 4) Level shift circuit built-in.
- 5) Thermal shut down circuit built-in.
- 6) Standby mode built-in.
- 7) **Dual actuator drivers:**
The drivers use current feedback to minimize the current phase shift caused by the influence of the load inductance. The output structure are two power OPAMPS in bridge configuration.
- 8) **Sled motor driver:**
A general purpose input OP provides differential input for signal addition. The output structure are two power OPAMPS in bridge configuration.
- 9) **Loading driver:**
Single input linear BTL driver. The output structure are two power OPAMPS in bridge configuration.

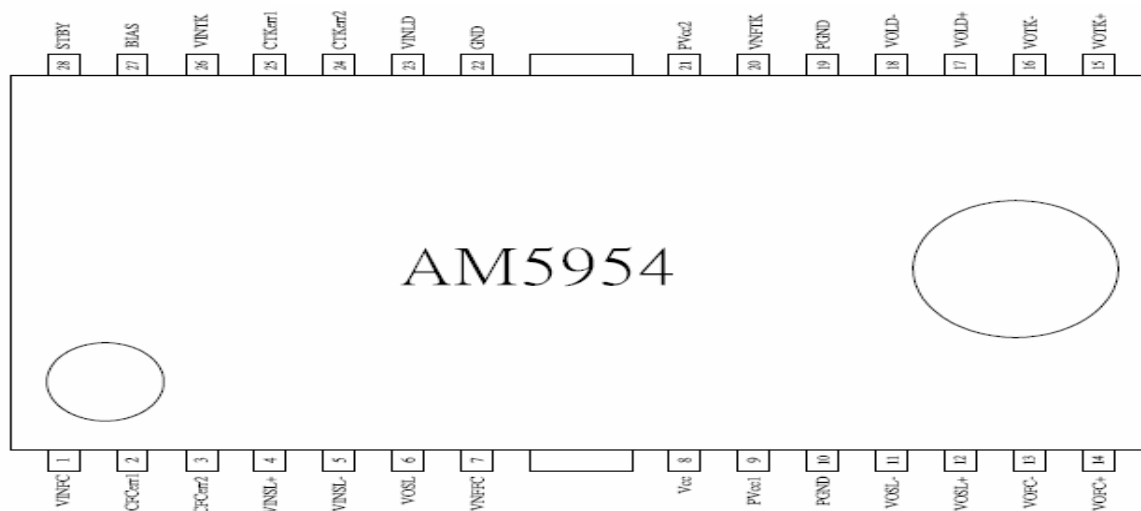
● Block diagram



● **Pin description**

PIN No	Pin Name	Function
1	VINFC	Input for focus driver
2	CFCerr1	Connection of capacitor for the error amp filter
3	CFCerr2	Connection of capacitor for the error amp filter
4	VINSL+	OPAMP input (+) for the sled driver
5	VINSL-	OPAMP input (-) for the sled driver
6	VOSL	OPAMP output for the sled driver
7	VNFFC	Focus driver feedback pin
8	Vcc	Vcc for pre-drive block and power block of sled
9	PVcc1	Vcc for power block of loading
10	PGND	GND for power block
11	VOSL-	Sled driver output (-)
12	VOSL+	Sled driver output (+)
13	VOFC-	Focus driver output (-)
14	VOFC+	Focus driver output (+)
15	VOTK+	Tracking driver output (+)
16	VOTK-	Tracking driver output (-)
17	VOLD+	Loading driver output (+)
18	VOLD-	Loading driver output (-)
19	PGND	GND for power block
20	VNFTK	Feedback for tracking driver
21	PVcc2	Vcc for power block of tracking and focus
22	GND	GND for pre-drive block
23	VINLD	Input for loading driver
24	CTKerr2	Connection of capacitor for the error amp filter
25	CTKerr1	Connection of capacitor for the error amp filter
26	VINTK	Input for tracking driver
27	BIAS	Input for reference voltage
28	STBY	Input for standby control

● **Pin configuration**



2. MT1389HD

Abbr. :

SR : Slew Rate

PU : Pull Up

PD : Pull Down

SMT : Schmitt Trigger

2MA~16MA : Output buffer driving strength.

Pin	Main	Alt.	Type	Description
RF Interface (26)				
231	RFGND18		Ground	Analog ground
232	RFVDD18		Power	Analog power 1.8V
252	OSP		Analog output	RF Offset cancellation capacitor connecting
253	OSN		Analog output	RF Offset cancellation capacitor connecting
254	RFGC		Analog output	RF AGC loop capacitor connecting for DVD-ROM
255	IREF		Analog Input	Current reference input. It generates reference current for RF path. Connect an external 15K resistor to this pin and AVSS.
256	AVDD3		Power	Analog power 3.3V
1	AGND		Ground	Analog ground
2	DVDA		Analog Input	AC coupled input path A
3	DVDB		Analog Input	AC coupled input path B
4	DVDC		Analog Input	AC coupled input path C
5	DVDD		Analog Input	AC coupled input path D
6	DVDRFIP		Analog Input	AC coupled DVD RF signal input RFIP
7	DVDRFIN		Analog Input	AC coupled DVD RF signal input RFIN
8	MA		Analog Input	DC coupled main-beam RF signal input A
9	MB		Analog Input	DC coupled main-beam RF signal input B
10	MC		Analog Input	DC coupled main-beam RF signal input C
11	MD		Analog Input	DC coupled main-beam RF signal input D
12	SA		Analog Input	DC coupled sub-beam RF signal input A
13	SB		Analog Input	DC coupled sub-beam RF signal input B
14	SC		Analog Input	DC coupled sub-beam RF signal input C
15	SD		Analog Input	DC coupled sub-beam RF signal input D
16	CDFON		Analog Input	CD focusing error negative input
17	CDFOP		Analog Input	CD focusing error positive input
18	TNI		Analog Input	3 beam satellite PD signal negative input
19	TPI		Analog Input	3 beam satellite PD signal positive input

ALPC (4)				
Pin	Main	Alt.	Type	Description
20	MDI1		Analog Input	Laser power monitor input
21	MDI2		Analog Input	Laser power monitor input
22	LDO2		Analog Output	Laser driver output
23	LDO1		Analog Output	Laser driver output

ADC Power (2)				
244	ADCVDD3		Power	Analog 3.3V Power for ADC
245	ADCVSS		Ground	Analog ground for ADC
VPLL (3)				
43	VPLLSS		Ground	Analog ground for VPLL
44	CAPPAD		Analog Input	VPLL External Capacitance connection
45	VPLLVD3		Power	Analog 3.3V Power for VPLL
Reference Voltage (3)				
28	V2REFO		Analog output	Reference voltage 2.8V
29	V20		Analog output	Reference voltage 2.0V
30	VREFO		Analog output	Reference voltage 1.4V
Analog Monitor Output (7)				
24	SVDD3		Power	Analog power 3.3V
25	CSO	RFOP	Analog output	1) 2) Central servo Positive main beam summing output
26	RFLVL	RFON	Analog output	1) 2) RFRP low pass, or Negative main beam summing output
27	SGND		Ground	Analog ground
31	FEO		Analog output	Focus error monitor output
32	TEO		Analog output	Tracking error monitor output
33	TEZISLV		Analog output	TE Slicing Level
Analog Servo Interface (6)				
246	RFVDD3		Power	Analog Power
247	RFRPDC		Analog output	RF ripple detect output
248	RFRPAC		Analog Input	RF ripple detect input(through AC-coupling)
249	HRFZC		Analog Input	High frequency RF ripple zero crossing
250	CRTPLP		Analog output	Defect level filter capacitor connecting
251	RFGND		Ground	Analog Power

RF Data PLL Interface (9)				
Pin	Main	Alt.	Type	Description
235	JITFO		Analog output	The output terminal of RF jitter meter.
236	JITFN		Analog Input	The input terminal of RF jitter meter.
237	PLLSS		Ground	Ground pin for data PLL and related analog circuitry.
238	IDACEXP		Analog output	Data PLL DAC Low-pass filter
239	PLLVD3		Power	Power pin for data PLL and related analog circuitry.
240	LPFON		Analog Output	The negative output of loop filter amplifier
241	LPFIP		Analog Input	The positive input terminal of loop filter amplifier.
242	LPFIN		Analog Input	The negative input terminal of loop filter amplifier.

243	LPFOP		Analog Output	The positive output of loop filter amplifier
Motor and Actuator Driver Interface (10)				
34	OP_OUT		Analog output	Op amp output.
35	OP_INN		Analog input	Op amp negative input
36	OP_INP		Analog input	Op amp positive input
37	DMO		Analog Output	Disk motor control output. PWM output.
38	FMO		Analog Output	Feed motor control. PWM output.
39	TROPENP W M		Analog Output	Tray PWM output / Tray open output.
40	PWMOUT 1	V_ADIN9	Analog Output	1) 1st General PWM output, or 2) Version AD input 9
41	TRO		Analog Output	Tracking servo output. PDM output of tracking servo compensator.
42	FOO		Analog Output	Focus servo output. PDM output of focus servo compensator
50	FG (Digital pin)	V_ADIN8	LVTTL 3.3V Input, Schmitt Input, pull up , with analog input path for V_ADIN8	1) Motor Hall sensor input, or 2) Version AD input 8
General Power/Ground (18)				
55,93, 142,160, 174, 213	DVDD18		Power	1.8V power pin for internal digital circuitry
81,178	DVSS		Ground	1.8V Ground pin for internal digital circuitry
65,96,11 8, 131,145, 156, 170, 208	DVDD3		Power	3.3V power pin for internal digital circuitry
90, 148	DVSS		Ground	3.3V Ground pin for internal digital circuitry

Micro Controller and Flash Interface (48)				
Pin	Main	Alt.	Type	Description
62	HIGHA0		Input 2~16MA, SR PU	Microcontroller address 8
74	HIGHA1		Input 2~16MA, SR PU	Microcontroller address 9
73	HIGHA2		Input 2~16MA, SR PU	Microcontroller address 10

72	HIGHA3		Input 2~16MA, SR PU	Microcontroller address 11
71	HIGHA4		Input 2~16MA, SR PU	Microcontroller address 12
70	HIGHA5		Input 2~16MA, SR PU	Microcontroller address 13
69	HIGHA6		Input 2~16MA, SR PU	Microcontroller address 14
68	HIGHA7		Input 2~16MA, SR PU	Microcontroller address 15
89	AD7		Input 2~16MA, SR	Microcontroller address/data 7
86	AD6		Input 2~16MA, SR	Microcontroller address/data 6
85	AD5		Input 2~16MA, SR	Microcontroller address/data 5
84	AD4		Input 2~16MA, SR	Microcontroller address/data 4
83	AD3		Input 2~16MA, SR	Microcontroller address/data 3
82	AD2		Input 2~16MA, SR	Microcontroller address/data 2
80	AD1		Input 2~16MA, SR	Microcontroller address/data 1
79	AD0		Input 2~16MA, SR	Microcontroller address/data 0
92	IOA0		Input 2~16MA, SR PU	Microcontroller address 0 / IO

Pin	Main	Alt.	Type	Description
77	IOA1		Input 2~16MA, SR PU	Microcontroller address 1 / IO
56	IOA2		Input 2~16MA, SR PU	Microcontroller address 2 / IO

57	IOA3		Input 2~16MA, SR PU	Microcontroller address 3 / IO
58	IOA4		Input 2~16MA, SR PU	Microcontroller address 4 / IO
59	IOA5		Input 2~16MA, SR PU	Microcontroller address 5 / IO
60	IOA6		Input 2~16MA, SR PU	Microcontroller address 6 / IO
61	IOA7		Input 2~16MA, SR PU	Microcontroller address 7 / IO
67	A16		Output 2~16MA, SR	Flash address 16
91	A17		Output 2~16MA, SR	Flash address 17
63	IOA18		Input 2~16MA, SR SMT	Flash address 18 / IO
64	IOA19		Input 2~16MA, SR SMT	Flash address 19 / IO
75	IOA20		Input 2~16MA, SR SMT	Flash address 20 / IO
87	IOA21		Input 2~16MA, SR SMT	1) Flash address 21 / IO 2) While External FLASH size <= 2MB: l) GPIO
88	ALE		Input 2~16MA, SR PU, SMT	Microcontroller address latch enable

Pin	Main	Alt.	Type	Description
78	IOOE#		Input 2~16MA, SR SMT	Flash output enable, active low / IO

66	IOWR#		Input 2~16MA, SR SMT	Flash write enable, active low / IO
76	IOCS#		Input 2~16MA, SR PU, SMT	Flash chip select, active low / IO
94	UWR#		Input 2~16MA, SR PU, SMT	Microcontroller write strobe, active low
95	URD#		Input 2~16MA, SR PU, SMT	Microcontroller read strobe, active low
97	UP1_2		Input 4MA, SR PU, SMT	Microcontroller port 1-2
98	UP1_3		Input 4MA, SR PU, SMT	Microcontroller port 1-3
99	UP1_4		Input 4MA, SR PU, SMT	Microcontroller port 1-4
100	UP1_5		Input 4MA, SR PU, SMT	Microcontroller port 1-5
101	UP1_6	SCL	Input 4MA, SR PU, SMT	1) Microcontroller port 1-6 2) I ² C clock pin
102	UP1_7	SDA	Input 4MA, SR PU, SMT	1) Microcontroller port 1-7 2) I ² C data pin
103	UP3_0	RXD	Input 4MA, SR PU, SMT	1) Microcontroller port 3-0 2) 8032 RS232 RXD
104	UP3_1	TXD	Input 4MA, SR PU, SMT	1) Microcontroller port 3-1 2) 8032 RS232 TXD
105	UP3_4	RXD SCL	Input 4MA, SR PU, SMT	1) Microcontroller port 3-4 2) Hardwired RD232 RXD 3) I ² C clock pin
106	UP3_5	TXD SDA	Input 4MA, SR PU, SMT	1) Microcontroller port 3-5 2) Hardwired RD232 TXD 3) I ² C data pin

109	IR		Input SMT	IR control signal input
110	INTO#		Input 4MA, SR PU, SMT	Microcontroller external interrupt 0, active low

Audio interface (28)					
Pin	Main	Alt.	Type	Description	
204	SPMCLK	SCLK0	Input Non-pull	1) 2)	Audio DAC master clock of SPDIF input While SPDIF input is not used: I) Serial interface port 0 clock pin II) GPIO
205	SPDATA	SDIN0	Input Non-pull	1) 2)	Audio data of SPDIF input While SPDIF input is not used: I) Serial interface port 0 data-in II) GPIO
206	SPLRCK	SDO0	Input Non-pull	1) 2)	Audio left/right channel clock of SPDIF input While SPDIF input is not used: I) Serial interface port 0 data-out II) GPIO
207	SPBCK	SDCS0 ASDATA5	Input Non-pull	1) 2)	Audio bit clock of SPDIF input While SPDIF input is not used: I) Serial interface port 0 chip select II) Audio serial data 5 part I : DSD data sub-woofer channel or Microphone output III) GPIO
209	ALRCK		Input 4MA, PD, SMT	1) 2)	Audio left/right channel clock Trap value in power-on reset: I) 1 : use external 373 II) 0: use internal 373
210	ABCK	Fs64	Output 4MA Non-pull	1) 2)	Audio bit clock Phase de-modulation
			Input		
211	ACLK		4MA		Audio DAC master clock
			Non-pull		

197	ASDATA0		Input 4MA PD SMT	1) 2) 3) 4)	Audio serial data 0 (Front-Left/Front-Right) DSD data left channel Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation While using external channels: I) GPO_2
202	ASDATA1		Input 4MA PD SMT	1) 2) 3) 4)	Audio serial data 1 (Left-Surround/Right-Surround) DSD data right channel Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation While using external channels: I) GPO_1
203	ASDATA2		Input 4MA PD SMT	1) 2) 3) 4)	Audio serial data 2 (Center/LFE) DSD data left surround channel Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation While using external channels: I) GPO_0
212	ASDATA3		Input 4MA PD SMT	1) 2) 3) 4)	Audio serial data 3 (Center-back/ Center-left-back/Center-right-back, in 6.1 or 7.1 mode) DSD data right surround channel Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation While only 2 channels output: I) GPO_0
214	ASDATA4	INT1#	Input 4MA PD SMT	1) 2) 3) 4)	Audio serial data 4 (Down-mixed Left/Right) DSD data center channel Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation While only 2 channels output: I) Microcontroller external interrupt 1 II) GPO_0
215	MC_DATA	INT2#	Input PD SMT	1) 2)	Microphone serial input While not support Microphone: I) Microcontroller external interrupt 2 II) GPO_0
216	SPDIF		Output 2~16MA, SR : ON/OFF Non-pull		SPDIF output

217	APLLVDD3		Power	3.3V Power pin for audio clock circuitry
218	APLLCAP		Analog Input	APLL External Capacitance connection

219	APLLVSS		Ground	Ground pin for audio clock circuitry
220	ADACVSS2		Ground	Ground pin for AUDIO DAC circuitry
221	ADACVSS1		Ground	Ground pin for AUDIO DAC circuitry
222	ARF	GPIO	Output	1) AUDIO DAC Sub-woofer channel output While internal 2) AUDIO DAC not used: GPIO
223	ARS	GPIO	Output	1) AUDIO DAC Right Surround channel output 2) While internal AUDIO DAC not used: a. SDATA3 b. GPIO
224	AR	GPIO	Output	1) AUDIO DAC Right channel output 2) While internal AUDIO DAC not used: a. SDATA1 b. GPIO
225	AVCM		Analog	AUDIO DAC reference voltage
226	AL	GPIO	Output	1) AUDIO DAC Left Surround channel output 2) While internal AUDIO DAC not used: a. SDATA2 b. GPIO
227	ALS	GPIO	Output	1) AUDIO DAC Left Surround channel output 2) While internal AUDIO DAC not used: a. SDATA0 b. GPIO
228	ALF	GPIO	Output	1) AUDIO DAC Center channel output 2) While internal AUDIO DAC not used:GPIO
229	ADACVDD1		Power	3.3V power pin for AUDIO DAC circuitry
230	ADACVDD2		Power	3.3V power pin for AUDIO DAC circuitry

Video Interface (18)

196	DACVDDC		Power	3.3V power pin for VIDEO DAC circuitry
195	VREF		Analog	Bandgap reference voltage
194	FS		Analog	Full scale adjustment
193	YUV0	CIN	Output 4MA, SR	1) Video data output bit 0 2) Compensation capacitor
192	DACVSSC		Ground	Ground pin for VIDEO DAC circuitry
191	YUV1	Y	Output 4MA, SR	1) Video data output bit 1 2) Analog Y output
190	DACVDDDB		Power	3.3V power pin for VIDEO DAC circuitry
189	YUV2	C	Output 4MA, SR	1) Video data output bit 2 2) Analog chroma output
188	DACVSSB		Ground	Ground pin for VIDEO DAC circuitry
187	YUV3	CVBS	Output 4MA, SR	1) Video data output bit 3 2) Analog composite output

186	DACVDDA		Power	3.3V power pin for VIDEO DAC circuitry
185	YUV4	Y/G	Output 4MA, SR	1) Video data output bit 4 2) Green or Y
184	DACVSSA		Ground	Ground pin for VIDEO DAC circuitry
183	YUV5	B/Cb/Pb	Output 4MA, SR	1) Video data output bit 5 2) Blue or CB

182	YUV6	R/Cr/Pr	Output 4mA, SR	1) Video data output bit 6 2) Red or CR
181	VSYN	V_ADIN1	Input 4mA, SR SMT Non-pull	1) Vertical sync input/output 2) While no External TV-encoder: I) Vertical sync for video-input II) Version AD input port 1 III) GPIO
180	YUV7	INT3# ASDATA5	Input 4mA, SR SMT Non-pull	1) Video data output bit 7 2) While no External TV-encoder: I) Microcontroller external interrupt 3 II) Audio serial data 5 part II : DSD data sub-woofer channel or Microphone output III) GPIO
179	HSYN	INT4# V_ADIN2	Input 4mA, SR SMT Non-pull	1) Horizontal sync input/output 2) While no External TV-encoder: I) Horizontal sync for video-input II) Microcontroller external interrupt 4 III) Version AD input port 2 IV) GPIO
MISC (12)				
46	USB_VSS		USB Ground	USB ground pin
47	USBP		Analog Input	USB port DPLUS analog pin
48	USBM		Analog Input	USB port DMINUS analog pin
49	USB_VDD3		USB Power	USB Power pin 3.3V
108	PRST#		Input PU, SMT	Power on reset input, active low
107	ICE		Input PD, SMT	Microcontroller ICE mode enable
233	XTALO		Output	27M crystal out
234	XTALI		Input	27M crystal in
201	GPIO_3		Input Pull-Down	GPIO
200	GPIO_4		Input Pull-Down	GPIO
199	RCLKB	GPIO_5	Input Pull-Up	GPIO
198	RVREF	GPIO_6	Input Pull-Up	GPIO

Dram Interface (58) (Sorted by position)				
176	C_0	IO_0 (RD16)	Input Non-pull	1) Digital Video output C bit 0 2) GPIO
175	C_1	IO_1 (RD17)	Input Non-pull	1) Digital Video output C bit 1 2) GPIO
173	C_2	IO_2 (RD18)	Input Non-pull	1) Digital Video output C bit 2 2) GPIO
172	C_3	IO_3 (RD19)	Input Non-pull	1) Digital Video output C bit 3 2) GPIO
171	C_4	IO_4 (RD20)	Input Non-pull	1) Digital Video output C bit 4 2) GPIO

169	C_5	IO_5 (RD21)	Input Non-pull	1) Digital Video output C bit 5 2) GPIO
168	C_6	IO_6 (RD22)	Input Non-pull	1) Digital Video output C bit 6 2) GPIO
167	C_7	IO_7 (RD23)	Input Non-pull	1) Digital Video output C bit 7 2) GPIO

177	IO_17	(DQM2)	Input Non-pull	GPIO
166	YUVCLK	IO_8 (DQM3)	Input Non-pull	1) Digital Video output Clock 2) GPIO
165	Y_0	IO_9 (RD24)	Input Non-pull	1) Digital Video output Y bit 0 2) GPIO
164	Y_1	IO_10 (RD25)	Input Non-pull	1) Digital Video output Y bit 1 2) GPIO
163	Y_2	IO_11 (RD26)	Input Non-pull	1) Digital Video output Y bit 2 2) GPIO
162	Y_3	IO_12 (RD27)	Input Non-pull	1) Digital Video output Y bit 3 2) GPIO
161	Y_4	IO_13 (RD28)	Input Non-pull	1) Digital Video output Y bit 4 2) GPIO
159	Y_5	IO_14 (RD29)	Input Non-pull	1) Digital Video output Y bit 5 2) GPIO
158	Y_6	IO_15 (RD30)	Input Non-pull	1) Digital Video output Y bit 6 2) GPIO
157	Y_7	IO_16 (RD31)	Input Non-pull	1) Digital Video output Y bit 7 2) GPIO

155	RA4		Input	DRAM address 4
154	RA5		Input	DRAM address 5
153	RA6		Input	DRAM address 6
152	RA7		Input	DRAM address 7

151	RA8		Input	DRAM address 8
150	RA9		Input	DRAM address 9
149	RA11		Input Pull-Down	DRAM address bit 11
147	CKE		output	DRAM clock enable
146	RCLK		Input	Dram clock
144	RA3		Input	DRAM address 3
143	RA2		Input	DRAM address 2
141	RA1		Input	DRAM address 1
140	RA0		Input	DRAM address 0
139	RA10		Input	DRAM address 10
138	BA1		Input	DRAM bank address 1
137	BA0		Input	DRAM bank address 0
136	RCS#		output	DRAM chip select, active low
135	RAS#		output	DRAM row address strobe, active low

134	CAS#		output	DRAM column address strobe, active low
133	RWE#		output	DRAM Write enable, active low
132	DQM1		Input	Data mask 1
130	IO_18	(DQS1)	Input Non-pull	GPIO
129	RD8		Input	DRAM data 8
128	RD9		Input	DRAM data 9

127	RD10		Input	DRAM data 10
126	RD11		Input	DRAM data 11
125	RD12		Input	DRAM data 12
124	RD13		Input	DRAM data 13
123	RD14		Input	DRAM data 14
122	RD15		Input	DRAM data 15
121	RD0		Input	DRAM data 0
120	RD1		Input	DRAM data 1
119	RD2		Input	DRAM data 2
117	RD3		Input	DRAM data 3
116	RD4		Input	DRAM data 4
115	RD5		Input	DRAM data 5
114	RD6		Input	DRAM data 6
113	RD7		Input	DRAM data 7
112	IO_19	(DQS0)	Input Non-pull	GPIO
111	DQM0		Input	Data mask 0

JTAG Interface(4)					
51	TDI	V_ADIN4	Input Non-pull	1) 2) 3)	Serial interface port 3 data-out Version AD input port 4 GPIO
52	TMS	V_ADIN5	Input Non-pull	1) 2) 3)	Serial interface port 3 data-in Version AD input port 5 GPIO
53	TCK	V_ADIN6	Input Non-pull	1) 2) 3)	Serial interface port 3 clock pin Version AD input port 6 GPIO
54	TDO	V_ADIN7	Input Non-pull	1) 2) 3)	Serial interface port 3 chip-select Version AD input port 7 GPO

Note:

1. The Main column is the main function, Alt. Means alternative function.
2. The multi-function GPIO pins are set to green characters.
3. The video input port and external TV encoder mode can not both use CCIR-601 mode, at least one of them should be in CCIR-656 mode.
4. Following is a summary of modified pins.
 - (a) Pin 48, 49, 50, 51 are no longer for JTAG functions.
 - (b) V_ADIN0 and V_ADIN3 is not available.

3. 24C16

2-Wire Serial CMOS E²PROM 16k (2048 x 8)

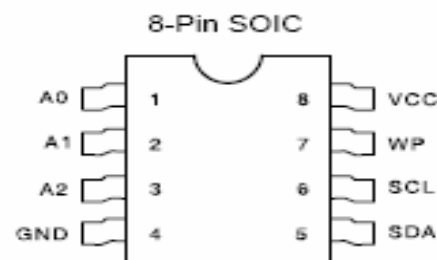
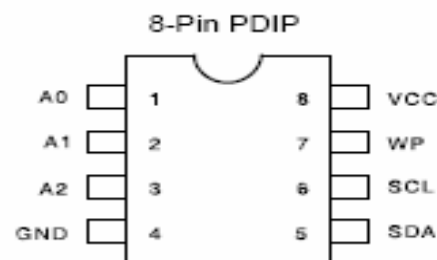
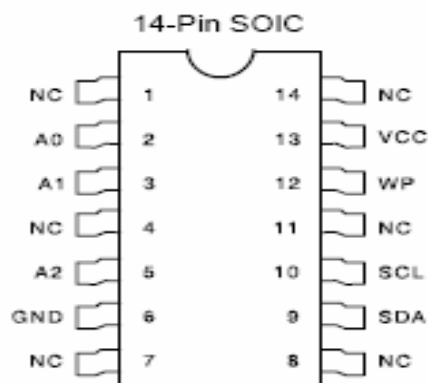
The AT24C16 provides 16384 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C16 is available in space saving 8-pin PDIP, 8-pin and 14-pin SOIC packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 5.0V(4.5V to 5.5V), 2.7V(2.7V to 5.5V) and 1.8V(1.8V to 5.5V) versions.

Features

- Low Voltage and Standard Voltage Operation
 - 5.0 (V_{CC} = 4.5V to 5.5V)
 - 2.7 (V_{CC} = 2.7V to 5.5V)
 - 2.5 (V_{CC} = 2.5V to 5.5V)
 - 1.8 (V_{CC} = 1.8V to 5.5V)
- Internally Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K) or 2048 x 8 (16K)
- 2-Wire Serial Interface
- Bidirectional Data Transfer Protocol
- 100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 8-Byte Page (1K, 2K), 16-Byte Page (4K, 8K, 16K) Write Modes
- Partial Page Writes Are Allowed
- Self-Timed Write Cycle (10 ms max)
- High Reliability
 - Endurance: 1 Million Cycles
 - Data Retention: 100 Years
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin and 14-Pin JEDEC SOIC and 8-Pin PDIP Packages

Pin Configurations

Pin Name	Function
A ₀ to A ₂	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect



Pin Capacitance ⁽¹⁾

Applicable over recommended operating range from $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$, $V_{CC} = +1.8\text{V}$.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O} = 0\text{V}$
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	6	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$, $T_{AC} = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$ (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.8		5.5	V
V_{CC2}	Supply Voltage		2.5		5.5	V
V_{CC3}	Supply Voltage		2.7		5.5	V
V_{CC4}	Supply Voltage		4.5		5.5	V
I_{CC}	Supply Current $V_{CC} = 5.0\text{V}$	READ at 100 kHz		0.4	1.0	mA
I_{CC}	Supply Current $V_{CC} = 5.0\text{V}$	WRITE at 100 kHz		2.0	3.0	mA
I_{SB1}	Standby Current $V_{CC} = 1.8\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}		0.6	3.0	μA
I_{SB2}	Standby Current $V_{CC} = 2.5\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}		1.4	4.0	μA
I_{SB3}	Standby Current $V_{CC} = 2.7\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}		1.6	4.0	μA
I_{SB4}	Standby Current $V_{CC} = 5.0\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}		8.0	18.0	μA
I_{LI}	Input Leakage Current	$V_{IN} = V_{CC}$ or V_{SS}		0.10	3.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or V_{SS}		0.05	3.0	μA
V_{IL}	Input Low Level ⁽¹⁾		-1.0		$V_{CC} \times 0.3$	V
V_{IH}	Input High Level ⁽¹⁾		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL2}	Output Low Level $V_{CC} = 3.0\text{V}$	$I_{OL} = 2.1\text{ mA}$			0.4	V
V_{OL1}	Output Low Level $V_{CC} = 1.8\text{V}$	$I_{OL} = 0.15\text{ mA}$			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$, $C_L = 1\text{ TTL Gate}$ and 100 pF (unless otherwise noted).

Symbol	Parameter	2.7-, 2.5-, 1.8-volt		5.0-volt		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		400	kHz
t_{LOW}	Clock Pulse Width Low	4.7		1.2		μs
t_{HIGH}	Clock Pulse Width High	4.0		0.6		μs
t_i	Noise Suppression Time ⁽¹⁾		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.1	0.9	μs
t_{BUF}	Time the bus must be free before a new transmission can start ⁽¹⁾	4.7		1.2		μs
$t_{HD,STA}$	Start Hold Time	4.0		0.6		μs
$t_{SU,STA}$	Start Set-up Time	4.7		0.6		μs
$t_{HD,DAT}$	Data In Hold Time	0		0		μs
$t_{SU,DAT}$	Data In Set-up Time	200		100		ns
t_R	Inputs Rise Time ⁽¹⁾		1.0		0.3	μs
t_F	Inputs Fall Time ⁽¹⁾		300		300	ns
$t_{SU,STO}$	Stop Set-up Time	4.7		0.6		μs
t_{DH}	Data Out Hold Time	100		50		ns
t_{WR}	Write Cycle Time		10		10	ms

Note: 1. This parameter is characterized and is not 100% tested.

4. NJM4558

DUAL OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

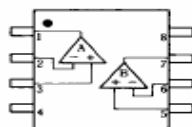
The NJM4558/4559 integrated circuit is a dual high-gain operational amplifier internally compensated and constructed on a single silicon chip using an advanced epitaxial process.

Combining the features of the NJM741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics. Excellent channel separation allow the use of the dual device in single NJM741 operational amplifier applications providing density. It is especially well suited for applications in differential-in, differential-out as well as in potentiometric amplifiers and where gain and phase matched channels are mandatory.

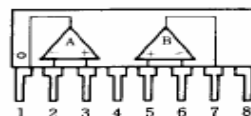
■ FEATURES

- Operating Voltage ($\pm 4V \sim \pm 18V$)
- High Voltage Gain (100dB typ.)
- High Input Resistance ($5M\Omega$ typ.)
- Package Outline DIP8, DMP8, SIP8, SSOP8
- Bipolar Technology

■ PIN CONFIGURATION



NJM4558D, NJM4558M, NJM4558V
NJM4559D, NJM4559M, NJM4559V



NJM4558L
NJM4559L

PIN FUNCTION

- 1.A OUTPUT
- 2.A -INPUT
- 3.A +INPUT
- 4.V-
- 5.B +INPUT
- 6.B -INPUT
- 7.B OUTPUT
- 8.V+

■ PACKAGE OUTLINE



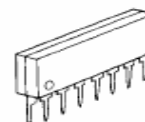
NJM4558D
NJM4559D



NJM4558M
NJM4559M



NJM4558V
NJM4559V



NJM4558L
NJM4559L

●Electrical characteristics (unless otherwise noted, $T_a = 25^\circ\text{C}$ and $V_{CC} = 9V$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output current	I_o	200	—	—	mA	
Output saturation voltage	V_{CE}	—	—	1.6	V	$I_o = 100\text{mA}$
Input high level voltage	V_{IH}	2.0	—	—	V	
Input low level voltage	V_{IL}	—	—	0.8	V	
Standby supply current	I_{ST}	—	—	0.4	mA	When inputs A and B are both LOW level
Input high level current	I_{IH}	—	—	400	μA	$V_{IH} = 4.5V$

A diode that absorbs at least 500 mA is built in to give protection against surge currents with a pulse width of 10 ms and a duty ratio of 10% or less.

5. BA033

Low saturation voltage type 3-pin regulator.

The BA00T and BA00FP series are fixed positive output low drop-out type, 3-pin voltage regulators with positive output. These regulators are used to provide a stabilized output voltage from a fluctuating DC input voltage. There are 10 fixed output voltages, as follows: 3V, 3.3V, 5V, 6V*, 7V, 8V, 9V, 10V, 12V and 15V. The maximum current capacity is 1A for each of the above voltages. (Items marked with an asterisk are under development.)

●Application

Constant voltage power supply

●Features

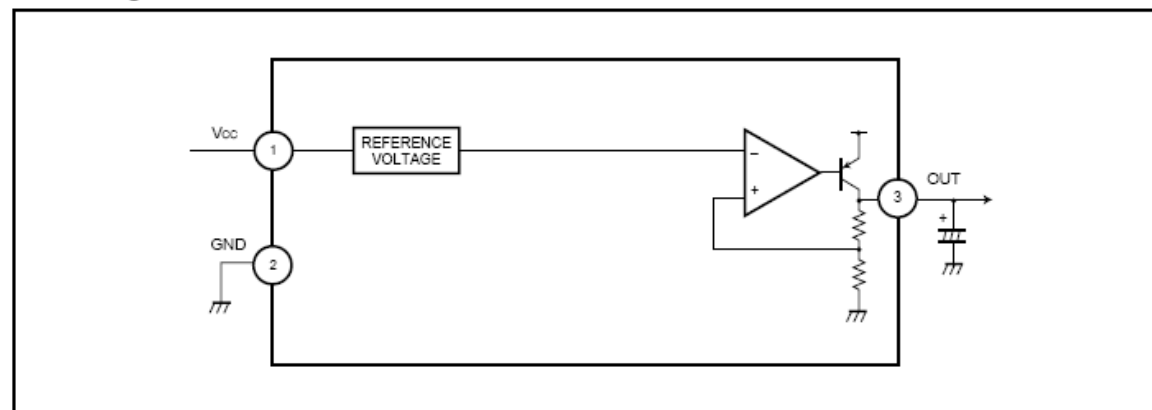
- 1) Built-in overvoltage protection circuit, overcurrent protection circuit and thermal shutdown circuit.
- 2) TO220FP and TO252-3 packages are available to cover a wide range of applications.
- 3) Compatible with the BA17800 series.
- 4) Richly diverse lineup.
- 5) Low minimum I / O voltage differential.

●Product codes

Output voltage (V)	Product No.	Output voltage (V)	Product No.
3.0	BA03T / FP	8.0	BA08T / FP
3.3	BA033T / FP	9.0	BA09T / FP
5.0	BA05T / FP	10.0	BA10T / FP
6.0	BA06T * / FP *	12.0	BA12T / FP
7.0	BA07T / FP	15.0	BA15T / FP

* : Under development.

●Block diagram



6. BA6287

The BA6287F is a reversible-motor driver with a maximum output current of 1.0A. Two logic inputs allow four output modes: forward, reverse, stop (idling), and brake. A built-in power saving circuit suppresses current consumption when the motor is in stop mode.

●Applications

VCRs and audio equipment in general

●Features

- 1) Built-in power saving circuit suppresses the stop mode current dissipation.
- 2) Output voltage can be set arbitrarily with the V_{REF} pin.
- 3) Interfaces with TTL devices.
- 4) Built-in thermal shutdown circuit.

●Absolute maximum ratings ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	18	V
Power dissipation	P_d	650*1	mW
Operating temperature	T_{opr}	$-20 \sim +75$	$^\circ\text{C}$
Storage temperature	T_{stg}	$-55 \sim +150$	$^\circ\text{C}$
Output current	$I_{o,max}$	1000*2	mA

* When mounted on a glass epoxy board (50 × 50 × 1.6 mm).

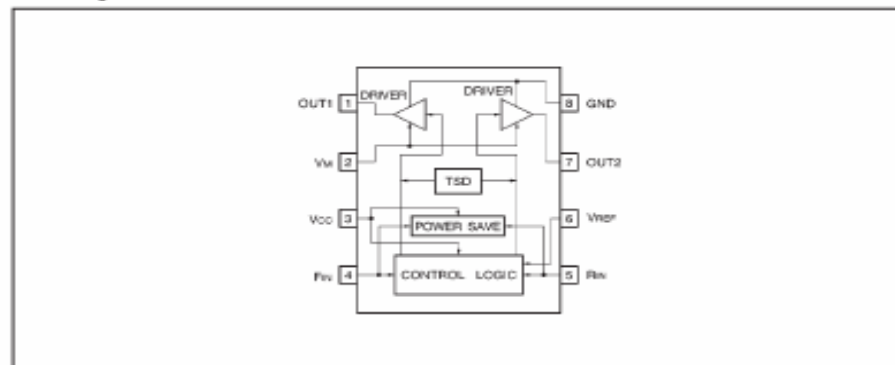
* 1 Reduced by 5.2 mW for each increase in T_a 1 $^\circ\text{C}$ over 25 $^\circ\text{C}$.

* 2 Should not exceed P_d or ASD values.

●Recommended operating conditions ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	4.5	—	15	V
Motor power supply voltage	V_M	4.5	—	15	V
Output high level voltage setting pin	V_{REF}	4.5	—	15	V

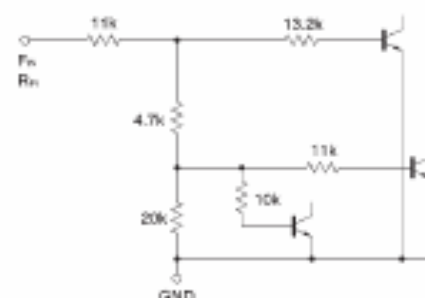
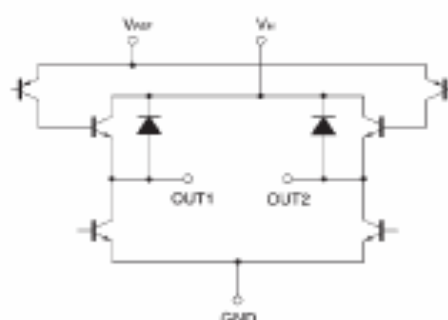
●Block diagram



●Pin descriptions

Pin No.	Pin name	Function
1	OUT1	Motor output
2	V_M	Motor power supply
3	V_{CC}	Power supply
4	F_v	Logic input
5	R_v	Logic input
6	V_{REF}	HIGH level output voltage setting
7	OUT2	Motor output
8	GND	GND

● Input / output circuits



● Electrical characteristics (unless otherwise noted, $T_a = 25^\circ\text{C}$, $V_{cc} = 9\text{V}$, $V_M = 9\text{V}$, $V_{KEP} = 9\text{V}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply current 1	I_{cc1}	12	24	36	mA	Forward or reverse mode
Supply current 2	I_{cc2}	29	48	67	mA	Brake mode
Standby supply current	I_{sr}	—	—	15	μA	Standby mode
V_{KEP} pin sink current	I_{KEP}	6	12	18	mA	Forward or reverse mode $I_O = 200\text{mA}$
Input high level voltage	V_{IH}	2.0	—	—	V	
Input low level voltage	V_{IL}	—	—	0.8	V	
Input high level current	I_{IH}	45	90	135	μA	$V_{IH} = 2.0\text{V}$
Output saturation voltage	V_{CE}	—	1.0	1.5	V	$I_O = 200\text{mA}$ Sum of output transistor high- and low-side voltages

● Circuit operation

(1) Input section

The four output modes are controlled by two logic inputs. Current flows from OUT1 to OUT2 when F_{IN} is HIGH and R_{IN} is LOW, and from OUT2 to OUT1 when R_{IN} is HIGH and F_{IN} is LOW (refer to the truth table). The input circuit can be operated by a logic circuit with a current capacity of 120 ~ 170 μA .

Input / output truth table

F_{IN}	R_{IN}	OUT1	OUT2	Mode
H	L	H	L	Forward
L	H	L	H	Reverse
H	H	L	L	Brake
L	L	OPEN	OPEN	Standby

(2) Output section

Current flows from OUT1 to OUT2 during forward rotation, and from OUT2 to OUT1 during reverse rotation. The output voltages V_{OH} and V_{OL} are given by :

$$V_{OH} [\text{V}] = V_{KEP} - V_{CE} (\text{sat}) (\text{PNP}) - V_{CE} (\text{NPN})$$

$$V_{OL} [\text{V}] = V_{CE} (\text{sat}) (\text{NPN})$$

V_{CE} and V_{KEP} are functions of the output current (see electrical characteristic curves). The output current can be set with the V_{KEP} pin.

(3) Power saving circuit

All circuits are turned OFF when the F_{IN} and R_{IN} input pins are both put to LOW level. This circuit saves power during standby mode by leaving the outputs OPEN.

(4) Thermal shutdown circuit

When the thermal shutdown circuit is activated at the chip temperature of about 175°C (typical), the outputs are left OPEN. The temperature difference between the activation and deactivation settings is about 15°C . When the thermal shutdown circuit is deactivated, the outputs revert to the status determined by input mode.

● Application example

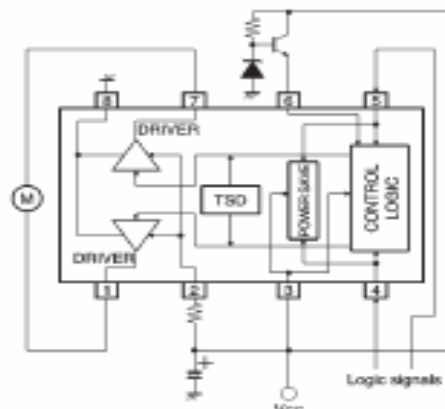


Fig. 1

● Operation notes

(1) The quality of these products have been carefully checked; however, use of the products with applied voltages, operating temperatures, or other parameters that exceed the absolute maximum rating given may result in the damage of the IC and the product it is used in. If the IC is damaged, the short mode and open modes cannot be specified, so if the IC is to be used in applications where parameters may exceed the absolute maximum ratings, then be sure to incorporate fuses, or other physical safety measures.

(2) GND potential

The potential for pin 1 must be kept lower than the potentials of the other pins regardless of the circumstances.

(3) Input pins

Voltage should never be applied to the input pins when the V_{cc} voltage is not applied to the IC. Similarly, when V_{cc} is applied, the voltage on each input pin should be less than V_{cc} and within the guaranteed range for the electrical characteristics.

(4) Back-rush voltage

Depending on the ambient conditions, environment, or motor characteristics, the back-rush voltage may fluctuate. Be sure to confirm that the back-rush voltage will not adversely affect the operation of the IC.

(5) Large current line

Large currents are carried by the motor power supply and motor ground for these ICs.

Therefore, the layout of the pattern of the PC board and the constants of certain parameters for external components, such as the capacitor between the power supply and ground, may cause this large output current to flow back to the input pins, resulting in output oscillation or other malfunctions. To prevent this, make sure that the PC board layout and external circuit constants cause no problems with the characteristics of these ICs.

(6) Power dissipation

The power dissipation will fluctuate depending on the mounting conditions of the IC and the ambient environment. Make sure to carefully check the thermal design of the application where these ICs will be used.

(7) Power consumption

The power consumption by the IC varies widely with the power supply voltage and the output current. Give full consideration to the power dissipation rating and the thermal resistance data and transient thermal resistance data, to provide a thermal design so that none of the ratings for the IC are exceeded.

(8) ASO

Make sure that the output current and supply voltage do not exceed the ASO values.

(9) Precautions for input mode switching

To ensure reliability, it is recommended that the mode switching for the motor pass once through the open mode.

(10) In-rush current

There are no circuits built into these ICs that prevent in-rush currents. Therefore, it is recommended to place a current limiting resistor or other physical countermeasure.

(11) Factors regarding the thermal, power supply, and motor conditions

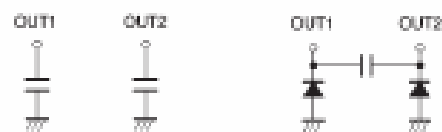
If the potential of the output pin sways greatly and goes below the potential of ground, the operation of the IC may malfunction or be adversely affected. In such a case, place a diode between the output and ground, or other measure, to prevent this.

(12) HIGH level output voltage setting pin

Ensure that the voltage applied to V_{HIGH} does not exceed the voltage on the motor power supply pin or the V_{cc} pin.

(13) The input pins have temperature-dependent characteristics. Take the temperature effect into consideration when using the IC.

(14) To eliminate motor noise, connect a capacitor between OUT1 and GND and between OUT2 and GND. Alternatively, connect a capacitor between OUT1 and OUT2, and also a diode between OUT1 and GND and between OUT2 and GND (see Fig. 2).



●Electrical characteristic curves

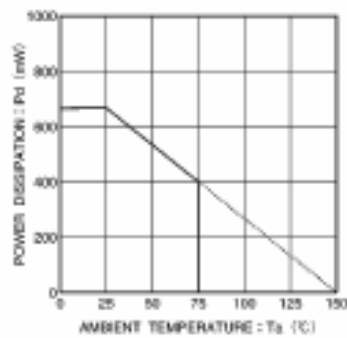


Fig.3 Thermal derating

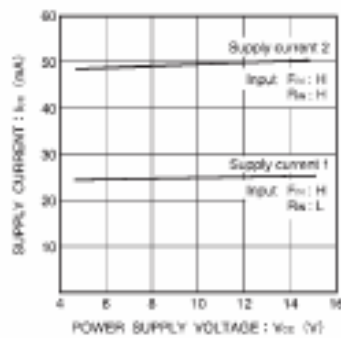


Fig.4 Supply current vs. power supply voltage

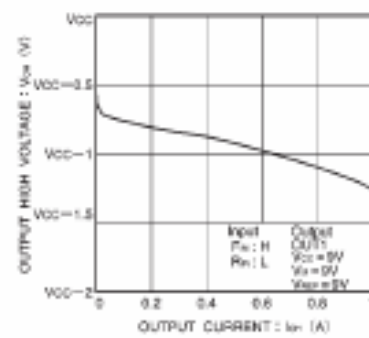


Fig.5 Output high level voltage vs. output current

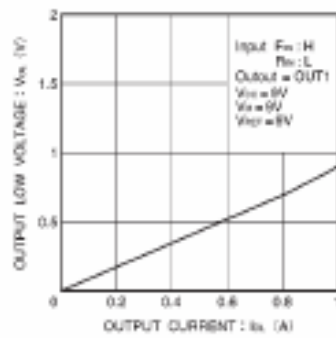


Fig.6 Output low level voltage vs. output current

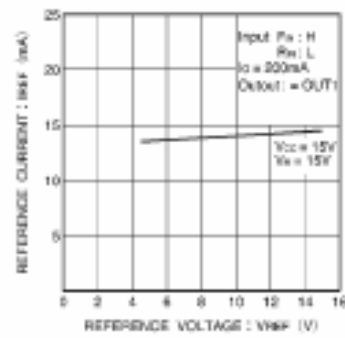


Fig.7 Vref reference current vs. Vref reference voltage

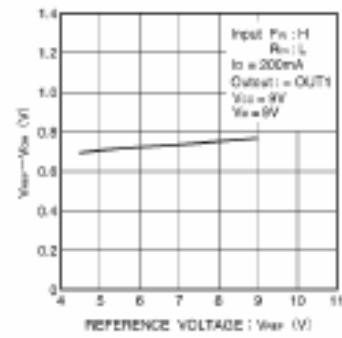
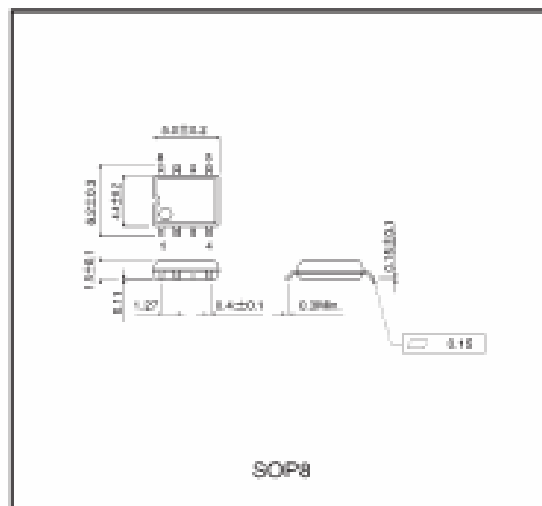
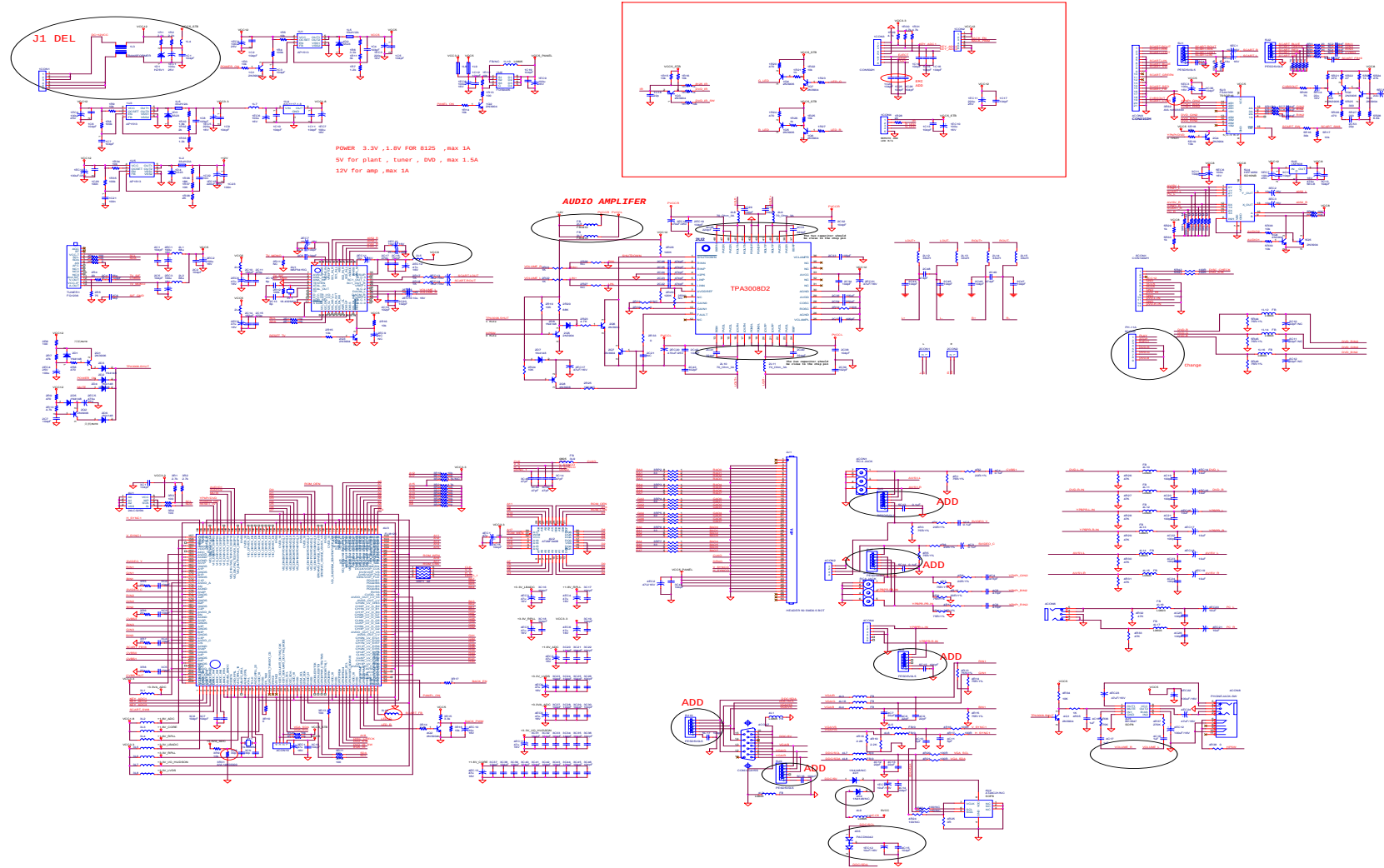


Fig.8 Vref-Voh voltage vs. Vref reference voltage

●External dimensions (Units: mm)



Part 4 Detailed Circuit MAIN BOARD



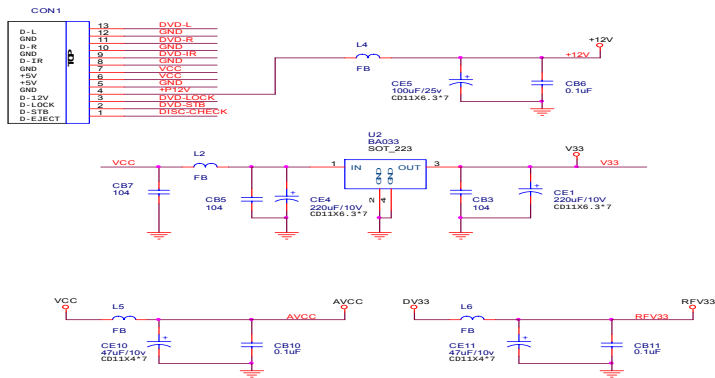
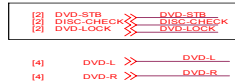
DVD BOARD

1. Index

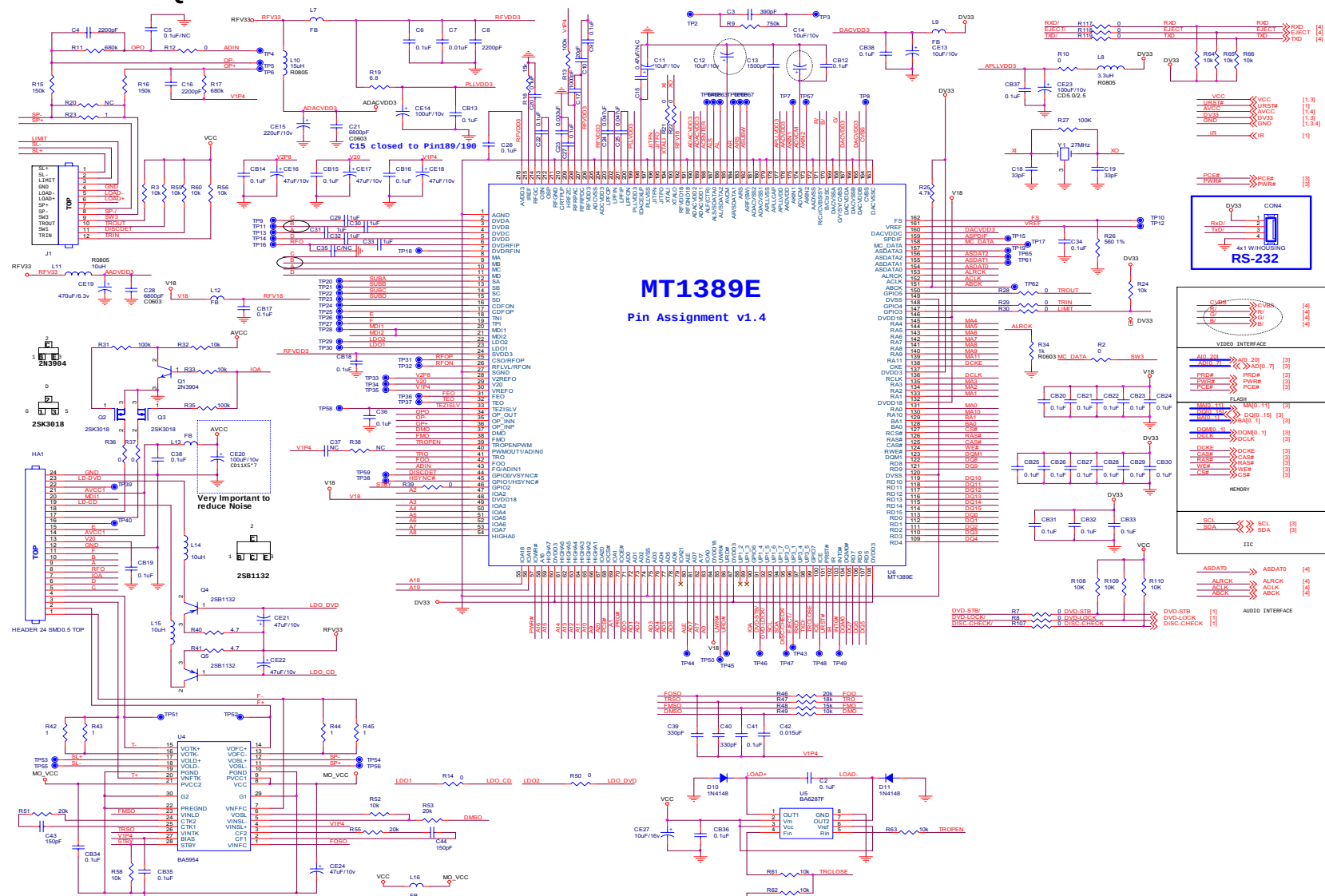
SLOTIN89E_ToHei_(TD-S208S-A62)
MT1389E (LQFP216) DVD MP Board for SANYO HD62PUH

- 1 INDEX & POWER, RESET
- 2 MT1389E
- 3 SDRAM & FLASH
- 4 VIDEO OUT & AV-CON
- 5 AUDIO OUT - CS4344

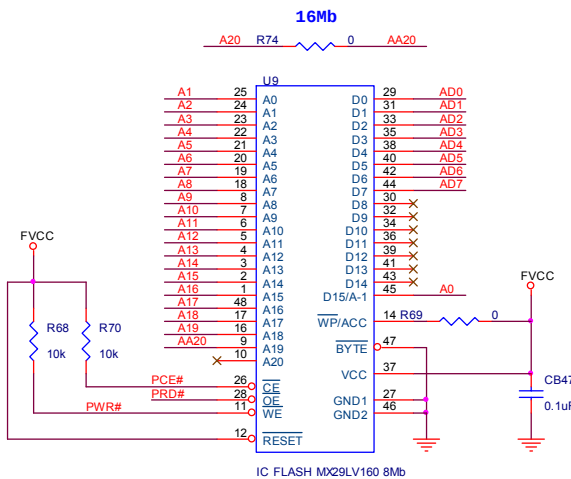
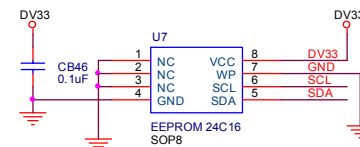
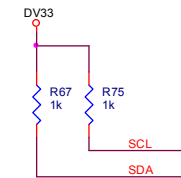
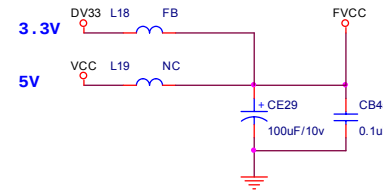
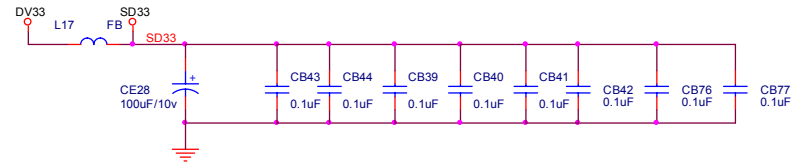
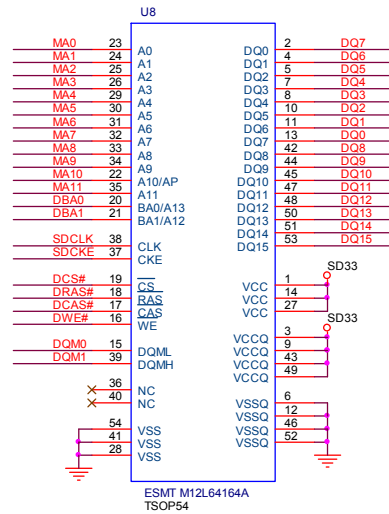
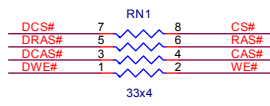
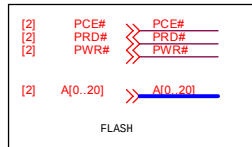
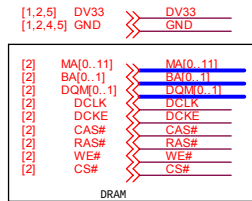
NAME	TYPE	DEVICE
VCC	Digital 5V	SUPPLY
DV33	Digital 3.3V	MT1389E
RFV33	Servo 3.3V	MT1389E
AV33	Laser Diode 3.3V	
V18	Digital 1.8V	MT1389E
SD33	Digital 3.3V	SDRAM
+12V	Audio +12V	OP AMP.
-12V	Audio -12V	OP AMP.
AVDD5	Audio 5V	Audio DAC
DVDD3	Audio 3.3V	Audio DAC



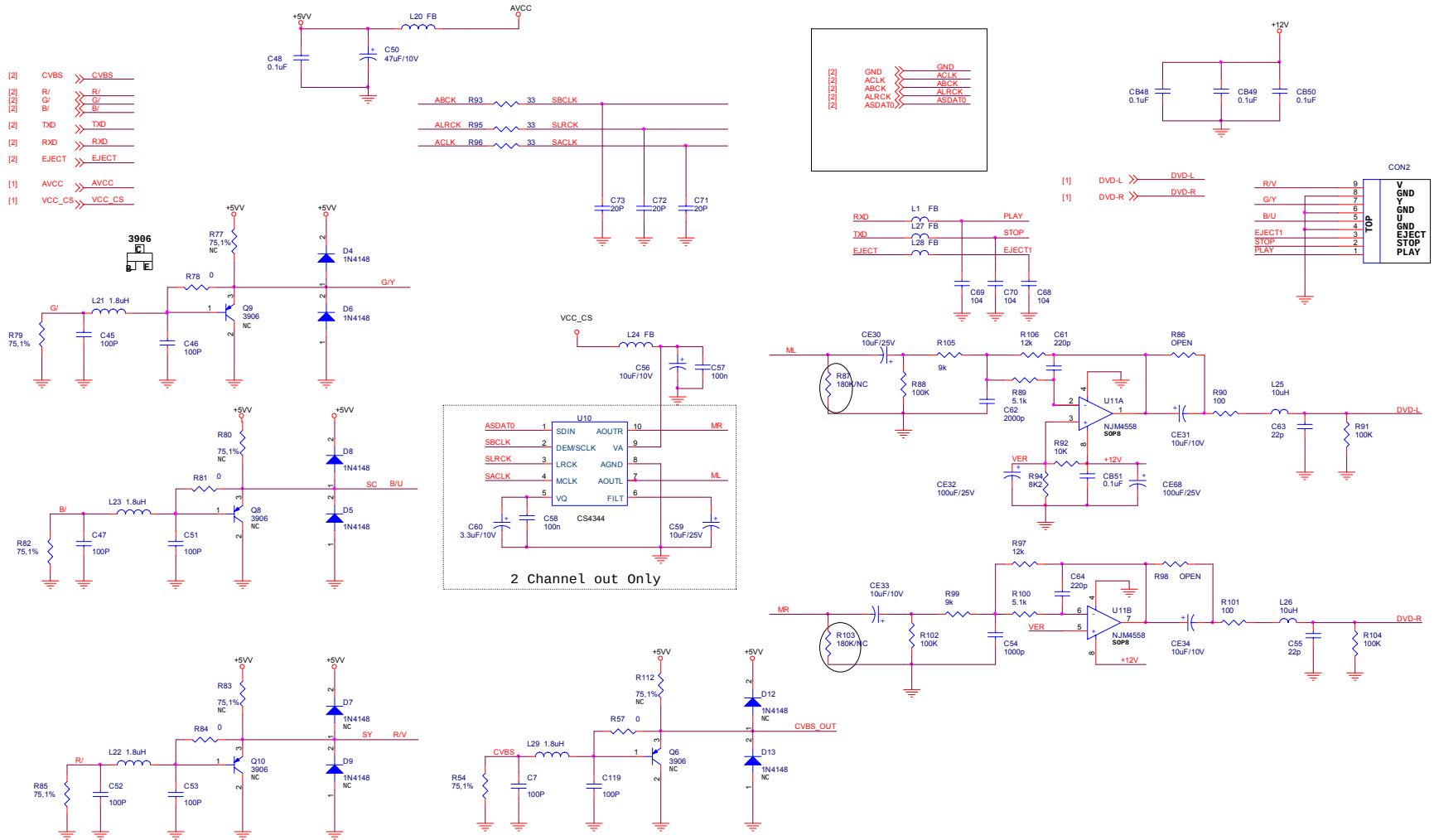
2. MT1389E LQFP 216



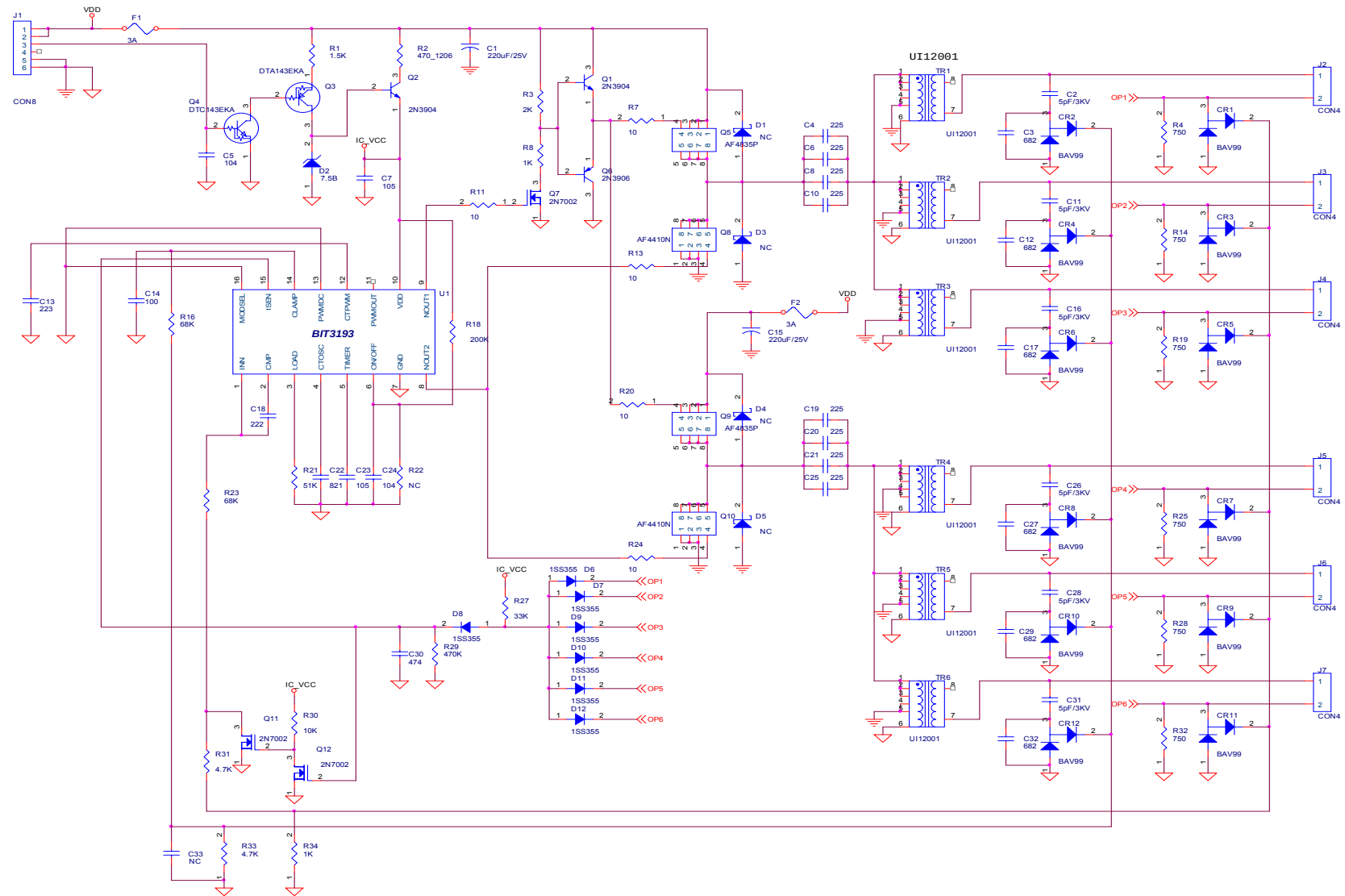
3. SDRAM & FLASH



4. VIDEO OUT & AV-CONNECTOR

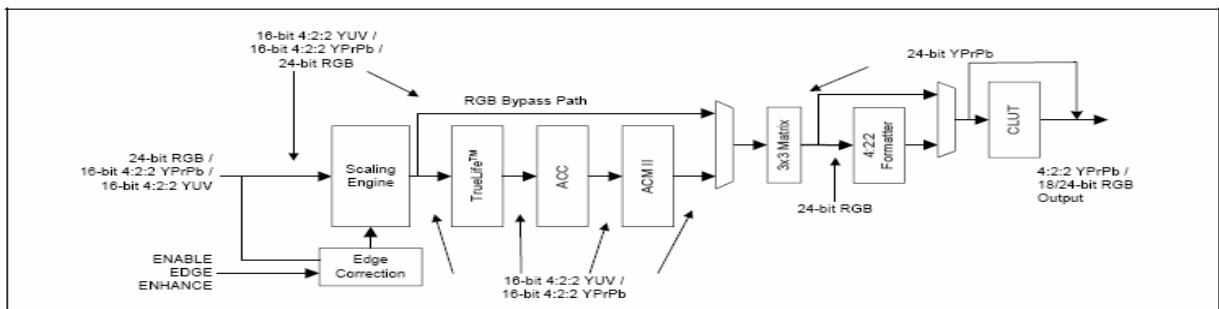
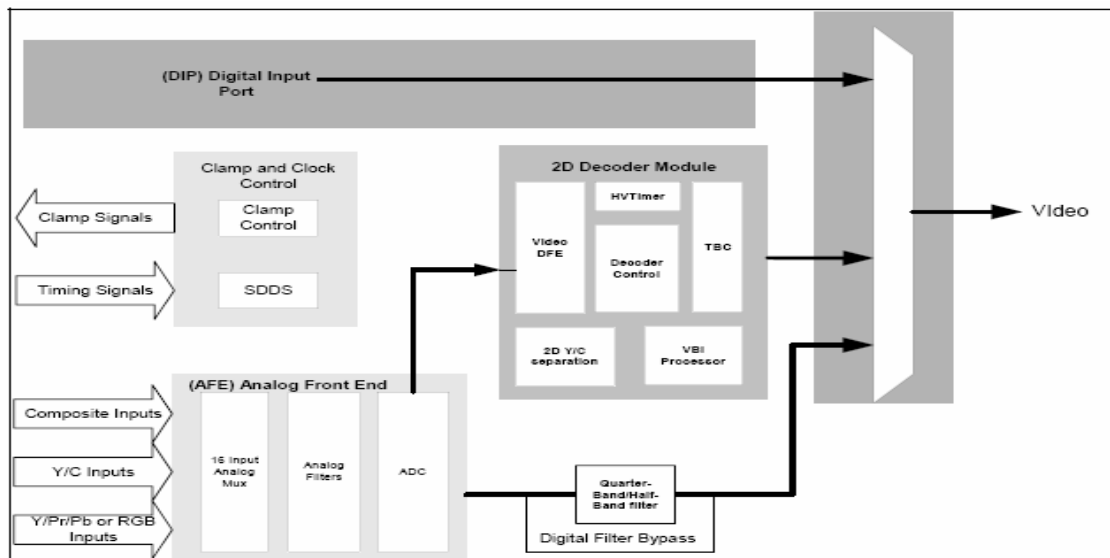
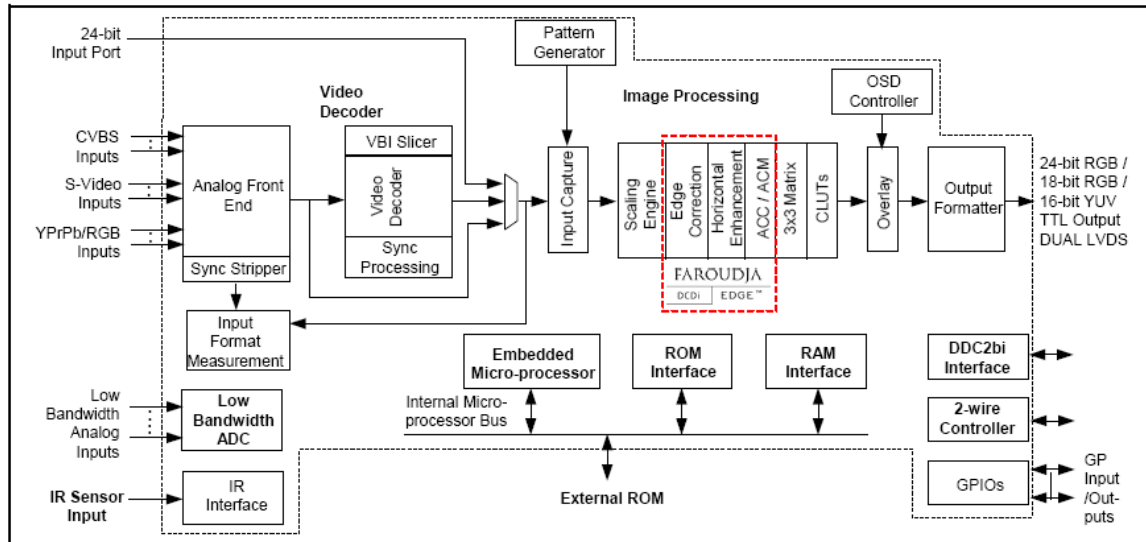


HI-VOLTAGE BOARD

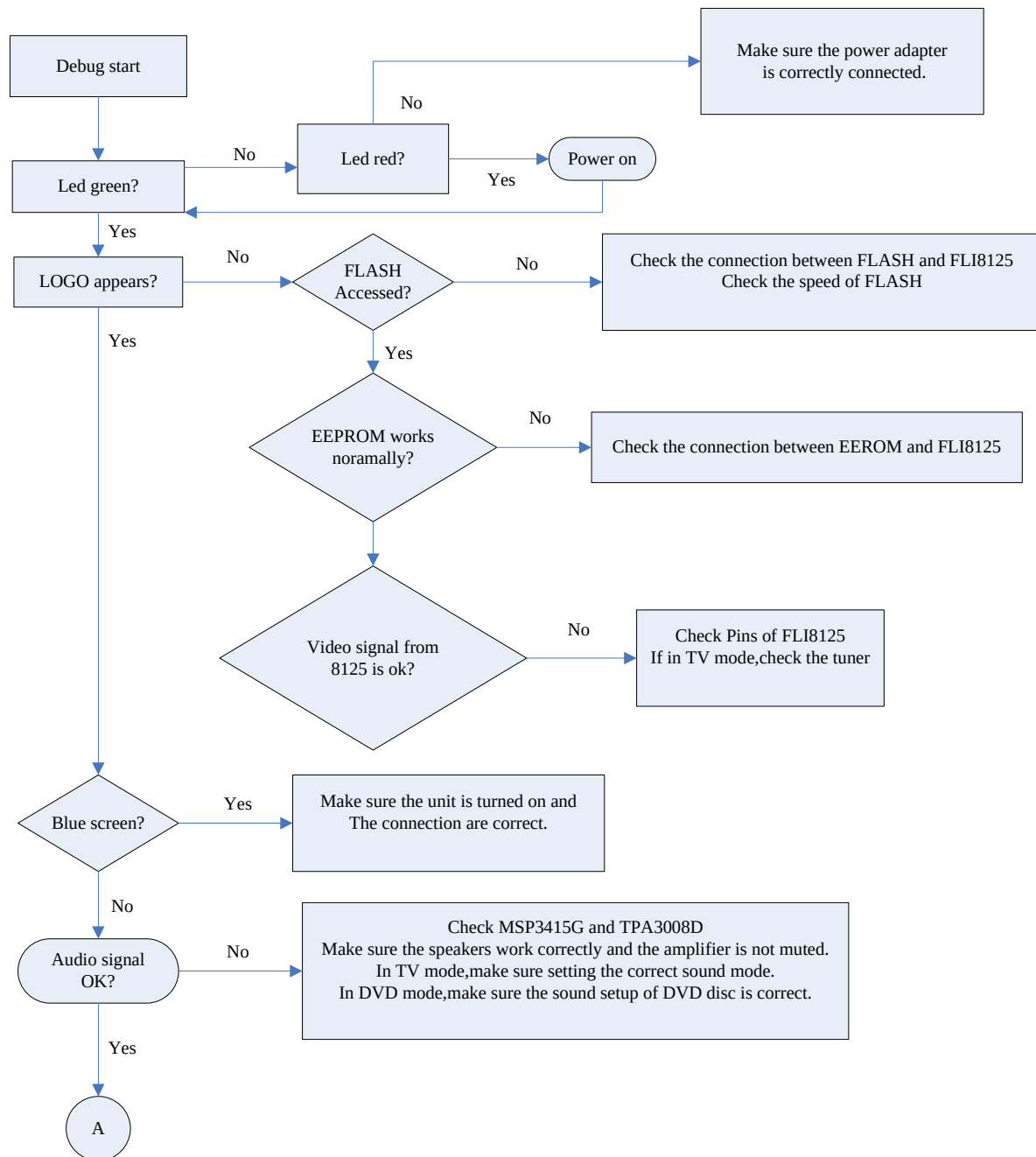


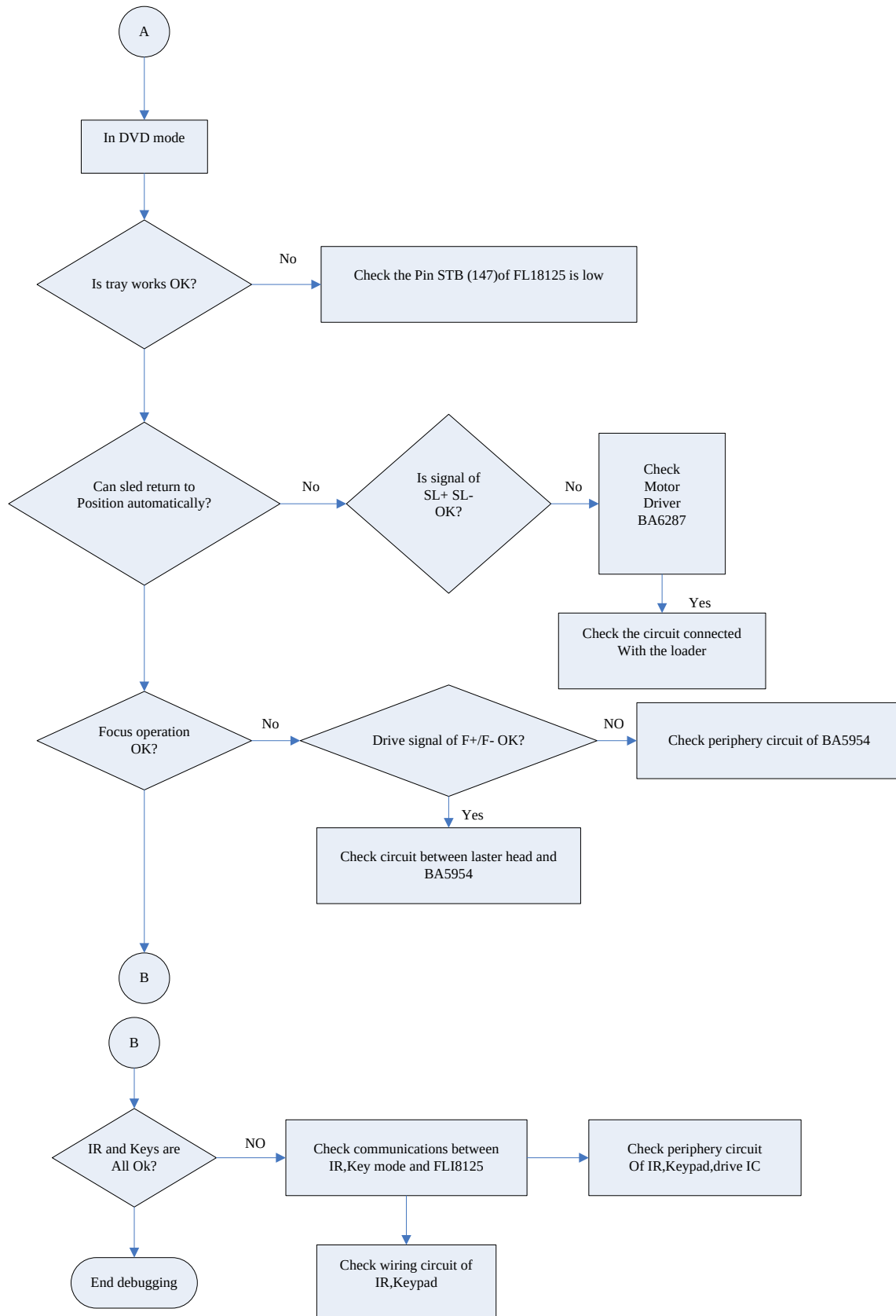
Part 5 Debugging Procedures

1. Signal process diagram



2. Debugging Strategy





3. Tips Of Some Typical Troubleshooting

White screen

First check voltage in HI-voltage Board; otherwise check the voltage of MAIN board , if abnormal , the problem occurs in 1U3. If the voltage is OK, check the LVDS. At last the connection between the main board and drive board may be the target for troubleshooting.

Black screen

This problem often arise from the voltage input to the screen, so the first step is to check the voltage of invert circuit. Otherwise check if the status is standby. If in TV mode, check the power for tuner is correct.

No color

Check if the connection with the external device is correct. Otherwise make sure the saturation is not zero. At last the problem may arise from the FLI8125.

Abnormal picture

Check if the range of the signal input to FLI8125 is correct. If no, the problem may be in the AFE(Analog Front End). Otherwise make sure the color system is correct. Then check the LVDS and the LCD Screen.

Pictures with no sound

Firstly, make sure the speakers works well. If so, the trouble mostly occurred in TDA3008D in 2U2 in main board, then MP3415G in 2U1.

Sounds with no picture

Check if any signal inputs to FLI8125, if yes, the problem may be in the AFE. Otherwise check the LVDS.